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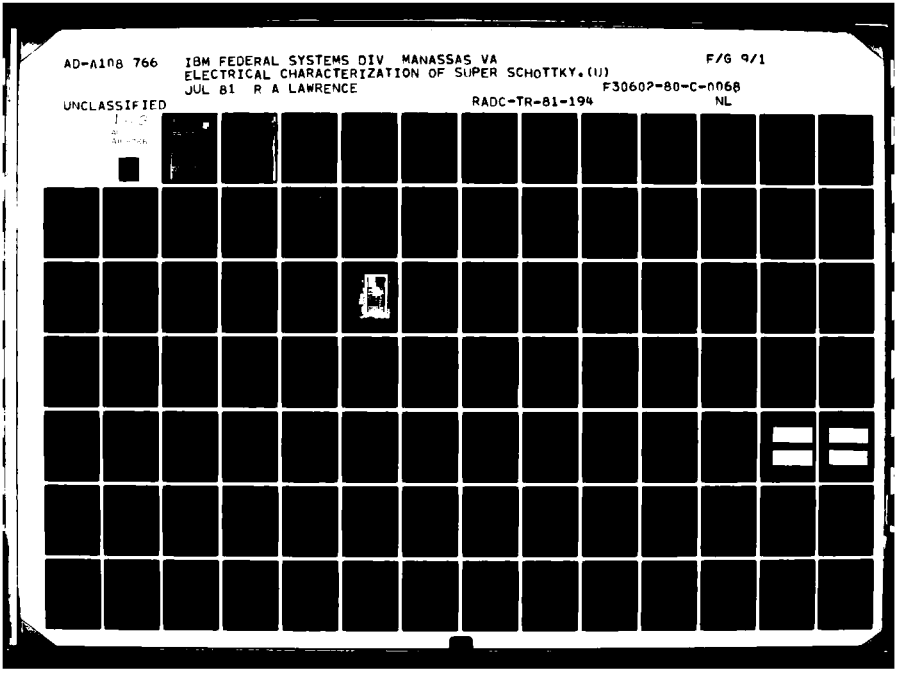

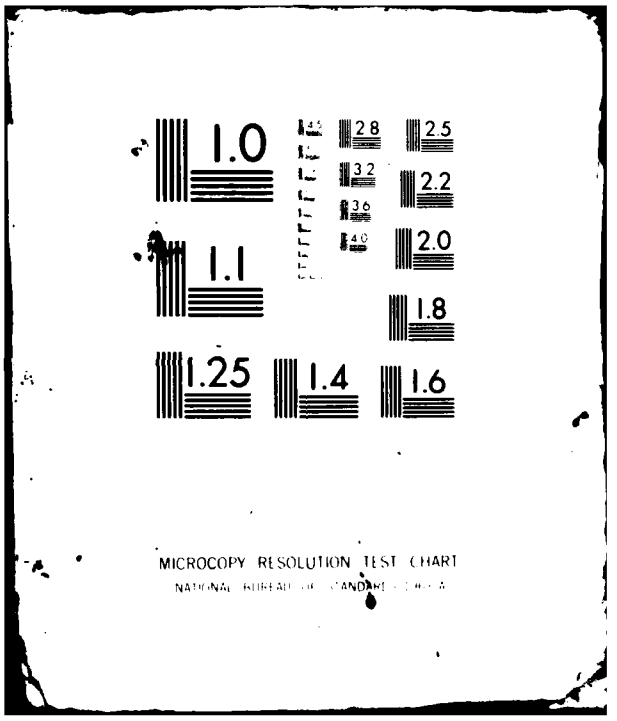
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RADC-TR-81-194
Final Technical Report
July 1981

LEVEL II (12)

ELECTRICAL CHARACTERIZATION OF SUPER SCHOTTKY

GM Corporation

A. Lawrence

229

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

State-of-the-art bipolar logic technology has advanced with the recent introduction of "Super Schottky" and "Low Power Super Schottky" product lines by two semiconductor manufacturers. Texas Instruments (T.I.) and Fairchild Semiconductor have utilized advances in processing techniques such as oxide isolation and refinements in the resolution of photolithographic equipment to enhance the speed and reduce the power of present day Schottky (S) and Low Power Schottky (LS) technologies. This report

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provides results obtained from the electrical characterization over the military temperature range (-55°CTj to + 125°CTj) of gate and flip-flop samples of three (3) new Transistor Transistor Logic (TTL) technologies; Advanced Schottky (AS), Advanced Low Power Schottky (ALS), and Fairchild Advanced Schottky (TTL) (FAST). This report shows that each technology offers the system designer unique advantages in terms of improved performance, power reductions, and space savings derived from functional design complexity. The performance improvements obtained by these new logic technologies, however, present implicit new application and testing considerations that could previously be ignored by the military system designer. The switching times (rise and fall times) achieved by the output transistors of Advanced Schottky circuits are approaching and in some cases equalling the propagation times of the signals through the wiring medium. This implies that transmission line effects must be considered in some applications, especially low-impedance wiring environments.

The characteristics of each technology are examined in this report, and application advantages and disadvantages are weighed. New testing techniques have been derived and recommended for each logic family evaluated, to provide a guide for future MIL-M-38510 detail specifications.

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Section 1
INTRODUCTION

This report summarizes the results of a technology evaluation study performed by the Logic Devices Department of IBM Federal System Division, Manassas, Virginia, under Rome Air Force Development Contract No. F30602-80-C-0068. This contract is entitled "Electrical Characterization of Super Schottky." The primary objectives of this contract are briefly outlined below:

Task 1: Select and procure representative gate and flip-flop samples of both Super Schottky and Low Power Super Schottky technologies from at least two (2) vendors for each technology.

Task 2: Electrically characterize gate and flip-flop samples of Super Schottky technology over the military temperature range. Document results in a final report and recommend electrical test procedures and characteristics for this technology that will be applicable to MIL-M-38510 specifications.

Task 3: Same as Task 2, but for Low Power Super Schottky technology.

Task 4: Present electrical performance trade-offs between different vendor designs of each technology.

1.1 BACKGROUND AND TECHNOLOGY DESCRIPTION

Before discussing test procedures and results, a brief definition and description of "Super Schottky" technology is in order. "Super Schottky" is an acronym given to a special family of twenty-eight (28) Schottky-clamped (54SS series) TTL devices developed between 1977 and 1979 for IBM by three semiconductor manufacturers, (Fairchild, Motorola, and Raytheon) specifically to meet the enhanced performance requirements of the NATO-E3A CC-2 computer. This family of parts achieved 50% speed improvement over equivalent Schottky (S) devices, (@ no load) with no increase over Schottky power. It exhibited

a speed/power product per gate of 66 pj (22mw x 3.0 ns). In the case of two vendors (Raytheon and Motorola) this speed improvement was achieved using conventional junction-isolation but taking advantage of advances in processing techniques such as ion-implantation and improvements in photolithographic equipment to construct smaller geometry transistors with shallower junctions (shallower than S or LS monolithic transistors). The third vendor Fairchild Semiconductor employed oxide-isolation along with the advanced processing techniques and equipment mentioned above, to achieve the reduction in transistor sizes and thus improve performance.

Although the three manufacturers of Super Schottky decided not to market this TTL circuit family outside of the NATO-E3A application, its very successful use on IBM's CC-2 Computer demonstrated its feasibility. This served as a stepping stone for leaders in the semiconductor industry to launch more attractive product lines that offer various advantages in speed and power over existing Schottky (S) and Low Power Schottky (LS) TTL circuit families. These manufacturers developed the capability to manipulate the switching speed and gain of a Schottky-clamped transistor, thereby controlling power. Switching speeds were enhanced by several means; thinner epitaxial layers, shallower diffusions or implantation depths, oxide-isolation, and walled bases and/or emitters. Transistor power was reduced because lower current levels were required to operate them.

Two distinct families of next generation bipolar logic technologies were considered in this study, power dissipation being the greatest distinction between them: (1) Super Schottky Family-Two product lines were originally proposed by IBM in order to meet the statement of work criteria of two vendors per family; Super Schottky, 54SSXX from Fairchild Semiconductor, and Advanced Schottky, 54ASXX from Texas Instruments (TI), (2) Low Power Super Schottky Family - Two product lines were proposed; 54FXX (Fairchild Advanced Schottky TTL), and 54ALSXX, Advanced Low Power Schottky from TI.

1.2 SUPER SCHOTTKY FAMILY - 54ASXX AND 54SSXX

Figures 1-1 and 1-2 schematically illustrate the circuit differences between the 54SS00 from Fairchild and the 54AS804 from T.I. The 54SS00 employs diode inputs for its AND function and the 54AS804 uses Titanium-Tungsten (Ti-W) Schottky diodes. The Ti-W Schottky diodes are used instead of a standard PN diode because of its fast switching speed and low forward voltage characteristic over temperature. A reasonably high input threshold of about 1.3 volts is achieved by both designs. Both circuits have two stages of transistor gain through Q2 & Q6 of the 54SS00, and Q1 & Q4 of the 54AS804. An output feedback diode scheme is employed in both circuits (D3 & D4 of the 54SS00 and D5 of the 54AS804) to speed-up TPHL delays by helping to discharge output load capacitance. Resistor values are also very similar.

Table 1-1 compares some pertinent input and output characteristics specified for the 54SSXX and 54ASXX families. As shown in Table 1-1, the AS product line offers 3 types of output drive characteristics, a Standard, a Buffer/3-State, and a Line Driver output. The 54SSXX family of parts had only one standard output configuration. The specified characteristics of the Standard AS input and output are very close to that of the 54SSXX.

Figures 1-3, 1-4, 1-5, and 1-6 compare some important D.C. characteristics of a 54SS00 from Fairchild and a 54AS804 and 54AS882 from TI. The 54AS804 represents a part with an AS Buffer output and the 54AS882 reprsents a part with an AS Standard output. Figure 1-3, I_{out} vs E_{out} (0), shows the presence of a feedback diode in each circuits output. This diode comes into play at $V_{OL} \geq 2.0$ volts on the output and increases output sink current depending on output voltage. The 54AS804, because it is a buffer, has an output sink capability of 52 mA at 0.5 volts which is higher than the 25 mA sink current at 0.5 volt of the 54SS00 and the 19.5 mA of the 54AS882. The 54SS00 would have equal or better sink capability than the 54AS804 if it were not for the high offset voltage or V_{SAT} of 0.3 volts at I_{out} = 0.0 mA.

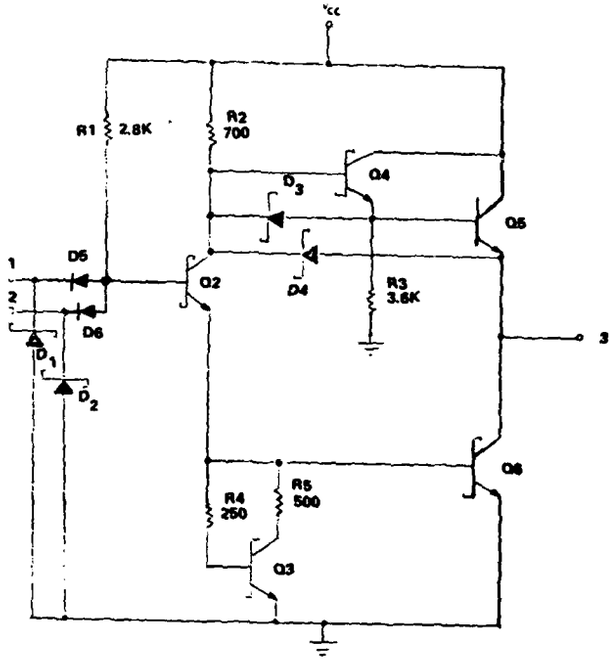


Figure 1-1. Basic Gate Design of the Super Schottky Family (54SS00)

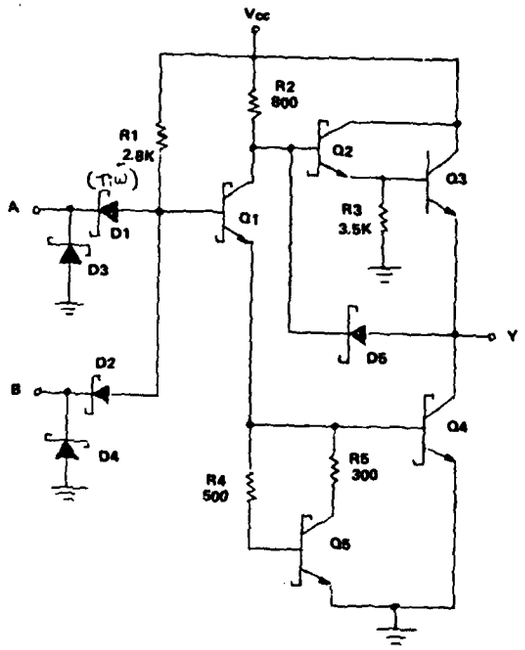


Figure 1-2. Basic Gate Design of the Super Schottky Family (54AS804)

Table 1-1. Specified Input/Output DC Characteristics of 54ASXX vs 54SSXX

Parameter	54ASXX			54SSXX	Unit
	Standard	Buffer/3-State	Line Driver	Standard	
Supply voltage	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	V
IOH	-2.0 max	-12.0 max	-40.0 max	-1.0 max	mA
V_{OH}	2.5 max	2.4 max	2.0 min	2.5 min	V
IOL	20.0 min	32.0 min	40.0 min	20.0 min	mA
V_{th}	1.3	1.3	1.3	1.3	V
I_{OS}	120 min	160 min	-200 min	-125 min	mA
I_{IL}	-2.0 max	-2.0 max	-2.0 max	-2.0	mA

NOTE: I_{OH} = High Level Output Current
V_{OH} = High Level Output Voltage @ I_{OH} Max, V_{CC} = 4.5 volts.
I_{OL} = Low Level Output Current @ V_{OL} = 0.5 volts, V_{CC} = 4.5 volts.
V_{th} = Input Threshold Voltage
I_{OS} = Output Short Circuit Current @ V_{OH} = 0.0 volts, V_{CC} = 5.5 volts.
I_{IL} = Low Level Input Current @ V_{IL} = 0.5 volts, V_{CC} = 5.5 volts.

The 54AS804 and the 54AS882 demonstrate superior driving capability to the logical '1' state in Figure 1-4. A difference in Darlington collector resistance and current gain allows the 54AS804 to source more current (≃ 240 mA) than the 54SS00 (150 mA) @ E_{out} (1) = 0.0 volts.

The input low-level load characteristic of the 54SS00 and the 54AS804 are very close as shown in the I_{IN} vs E_{IN} (0) plot in Figure 1-5 (1.7 mA and 1.5 mA @ 0.4 volts, respectively). This is consistent because input pull-up resistors are of similar value (R1 = 2.8 kΩ).

Figure 1-6 gives an indication of the DC power dissipation per gate of the AS and SS families. Keeping in mind that the 54AS804 has six gates and the 54SS00 four, each part type dissipates approximately the same power per gate, i.e., 26 mW/gate or 5.2 mA @ 5.0 volt V_{cc}.

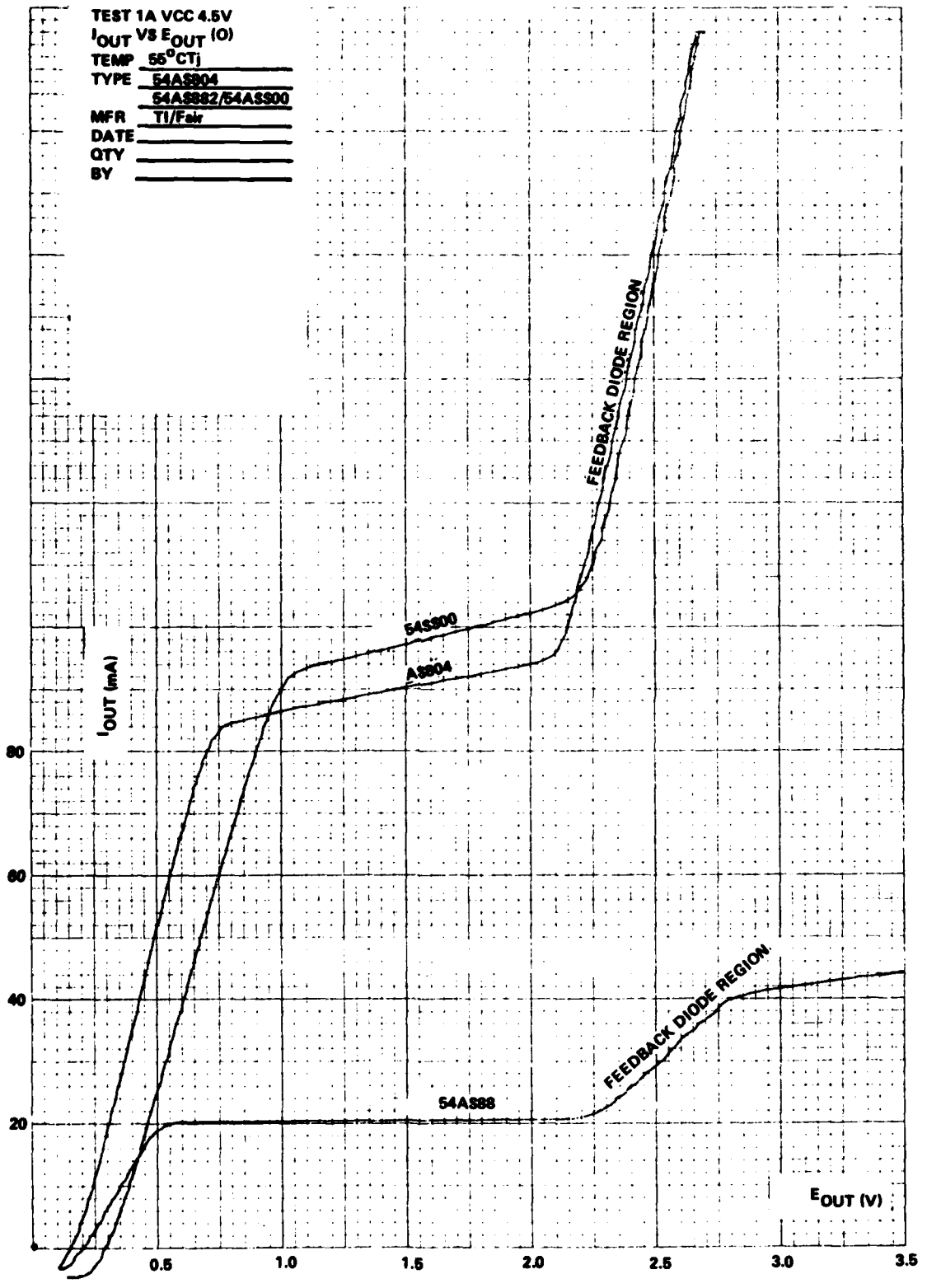


Figure 1-3. Super Schottky Technology I_{OUT} VS E_{OUT} (O)

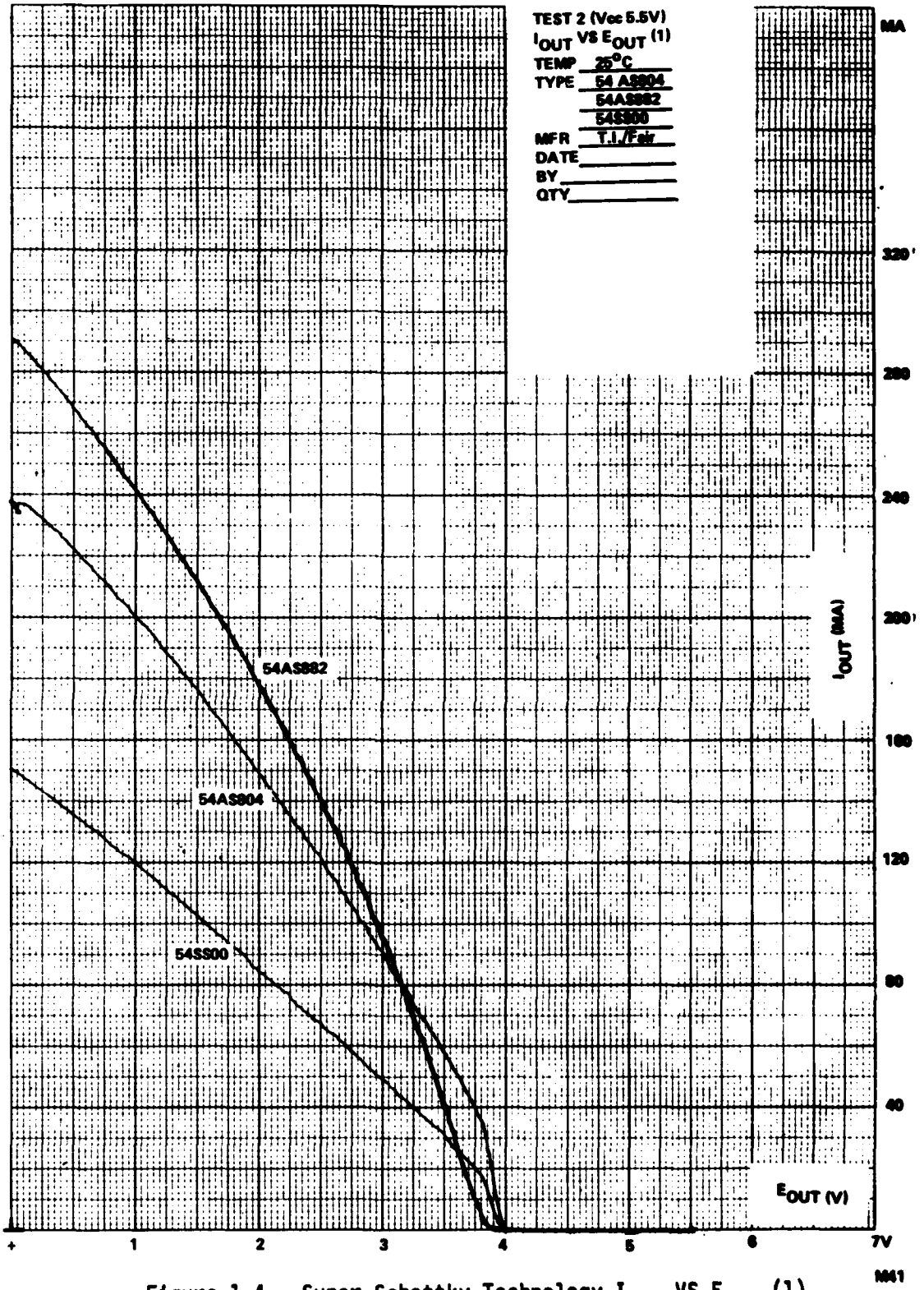


Figure 1-4. Super Schottky Technology I_{OUT} VS E_{OUT} (1)

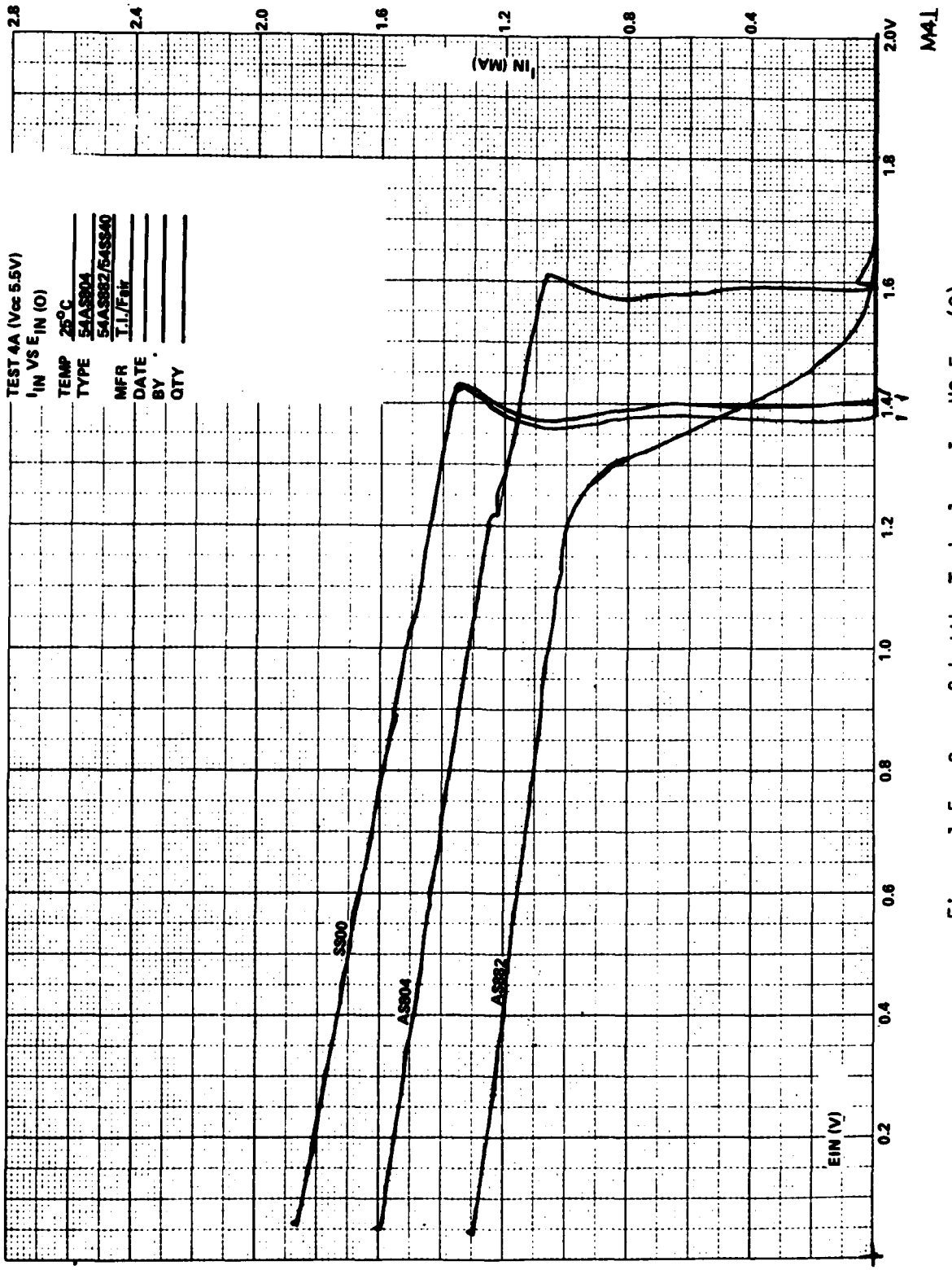


Figure 1-5. Super Schottky Technology I_{IN} VS E_{IN} (O)

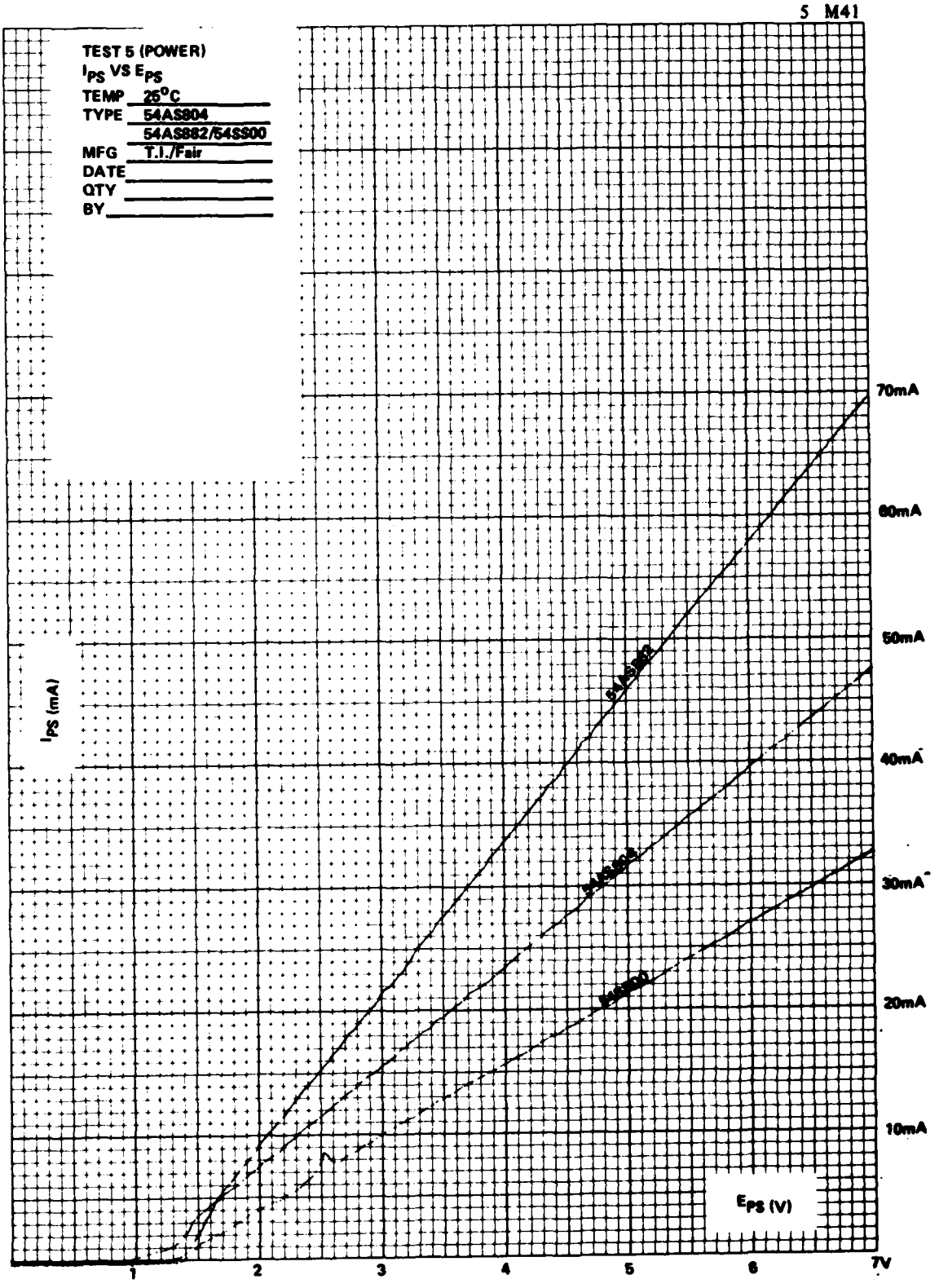


Figure 1-6. Super Schottky Technology I_{PS} VS E_{PS}

1.3 LOW POWER SUPER SCHOTTKY FAMILY - 54FXX and 54ALSXX

Figures 1-7 and 1-8 compare the basic gate design of 54ALS20 to that of a 54F20. The 54F20 employs diode inputs for its AND function, while the 54ALS20 uses high impedance, common collector, PNP transistor inputs. Both circuits use three stages of gain (Q6, Q5 & Q3) as compared with two stages of gain used in AS, and SS TTL designs. These designs raise the input threshold above those achievable with two stages of gain. FAST threshold is 1.5 volts at 25°C and ALS threshold is 1.3 volts at 25°C. The salient differences between the two technologies lie in resistor values and the sizes of diodes and transistors. Critical resistor values are typically four times larger on the ALS gate than on the FAST. Fairchild's use of a walled-emitter oxide-isolated process allows them to fabricate small devices with low sidewall capacitance. ALS power per gate is typically 1/2 to 1/3 that of FAST. ALS and FAST have quite different input and output DC characteristics as can be seen from the four DC plots in Figures 1-9 through 1-12 inclusive. Each family is clearly designed to interface with different logic technologies. The 54ALS20 does not have the drive capability of the 54F20 to the logical zero state as can be seen in the I_{out} VS E_{out} (0) plot in Figure 1-9. The ALS20 can drive 10 LS unit loads (.4 mA/unit load) to the logical zero state because its output meets the LS I_{OL} specification of 4 mA minimum @ 0.4 volts V_{OL}. However, the 54ALS20 cannot drive 10 Schottky unit loads (2 mA/unit load) to the logical zero state as can the 54F20. The 54F20 is specified to meet the Schottky driver requirements of I_{OL} = 20 mA minimum @ 0.5 volts, V_{OL}.

Both the 54F20 and the 54ALS20 have output feedback diodes which, when the output is switching low, will become forward-biased from the up level to 1.8 volts, providing additional base drive to the output transistor(s) (Q3, Figure 1-7 and 1-8) through the phase splitter(s) (Q5 Figures 1-7 and 1-8). This additional base drive increases output transistor's collector current depending on collector voltage (see feedback diode region of Figure 1-9).

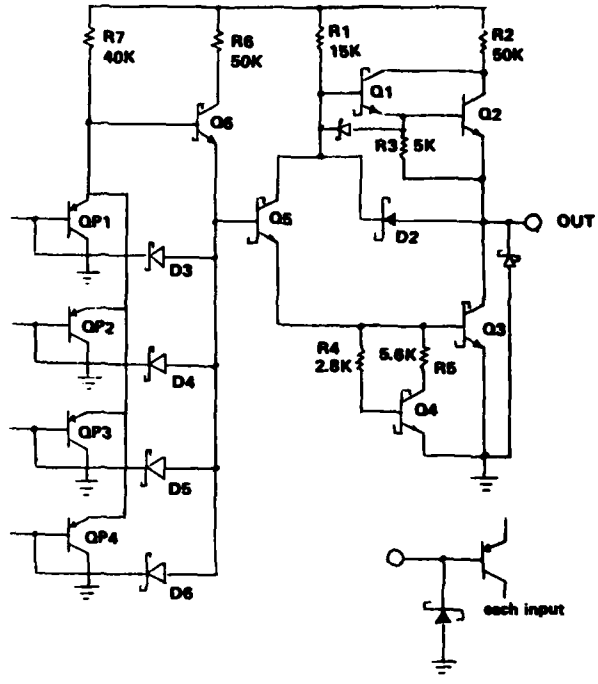


Figure 1-7. Basic Gate Design of the Low Power Super Schottky Family (54ALS20)

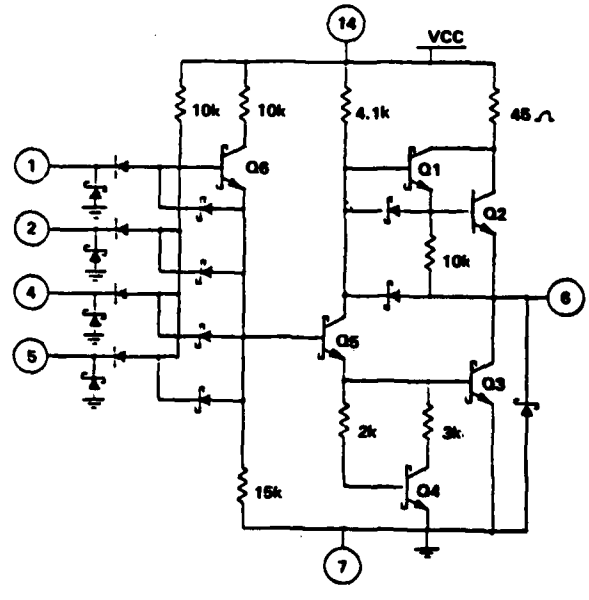


Figure 1-8. Basic Gate Design of the Low Power Super Schottky Family (54F20)

The output short circuit current, I_{OS}, of the 54F20 and the 54ALS20, on the other hand, are very close as evidenced in Figure 1-10 (95 mA and 85 mA, respectively). Both devices have similar Darlington transistor base-emitter characteristics because the outputs start to source current at about 4.0 volts with V_{cc} = 5.5 volts.

The power supply current plot in Figure 1-12 shows that the 54ALS20 dissipates approximately one third the power of the 54F20. At V_{cc} = 5.0 volts, the 54F20 draws 2.4 mA I_{cc}, while the 54ALS20 draws 0.8 mA. Differences between FAST and ALS are also conveyed in the I_{IN} vs E_{IN} (0) plot in Figure 1-11. The 54F20 requires the driving device to sink typically 0.34 mA @ 0.4 volts V_{IL}, whereas the 54ALS20, input low cur-rent is less than 20 µA @ 0.4 volts. Differences in performance will be discussed later in the summary of characterization results.

Another major difference between the ALS and FAST circuit families exsits in the design of flip-flop and 3-state circuits. FAST uses the enhanced drive feedback circuitry on all circuit outputs. ALS does not use feedback on flip-flop and 3-state outputs. Even though ALS 3-state outputs have higher, low output voltage sink currents than standard ALS outputs, the lack of enhanced high output voltage sink limits the load driving capability of 3-state ALS circuits. The lack of feedbacks on flip-flop outputs with the standard ALS drive results in even poorer load driving capability than 3-state outputs. This limitation will be discussed later in this report showing the undesirable, poor, low impedence, signal line driving capabilities of ALS flip-flop and 3-state circuits.

Table 1-2 compares some of the processing features of ALS, FAST, and AS. The significant difference between the processes is the walled emitters of Fairchild's oxide-isolated process. This feature permits the building of smaller transistors using equivalent lithography and registrations. The smaller transistors have low parasitic capacitances and high frequency responses. The low parasitic capacitances are especially important in low power circuits that use large value resistors so that RC time constants are minimized.

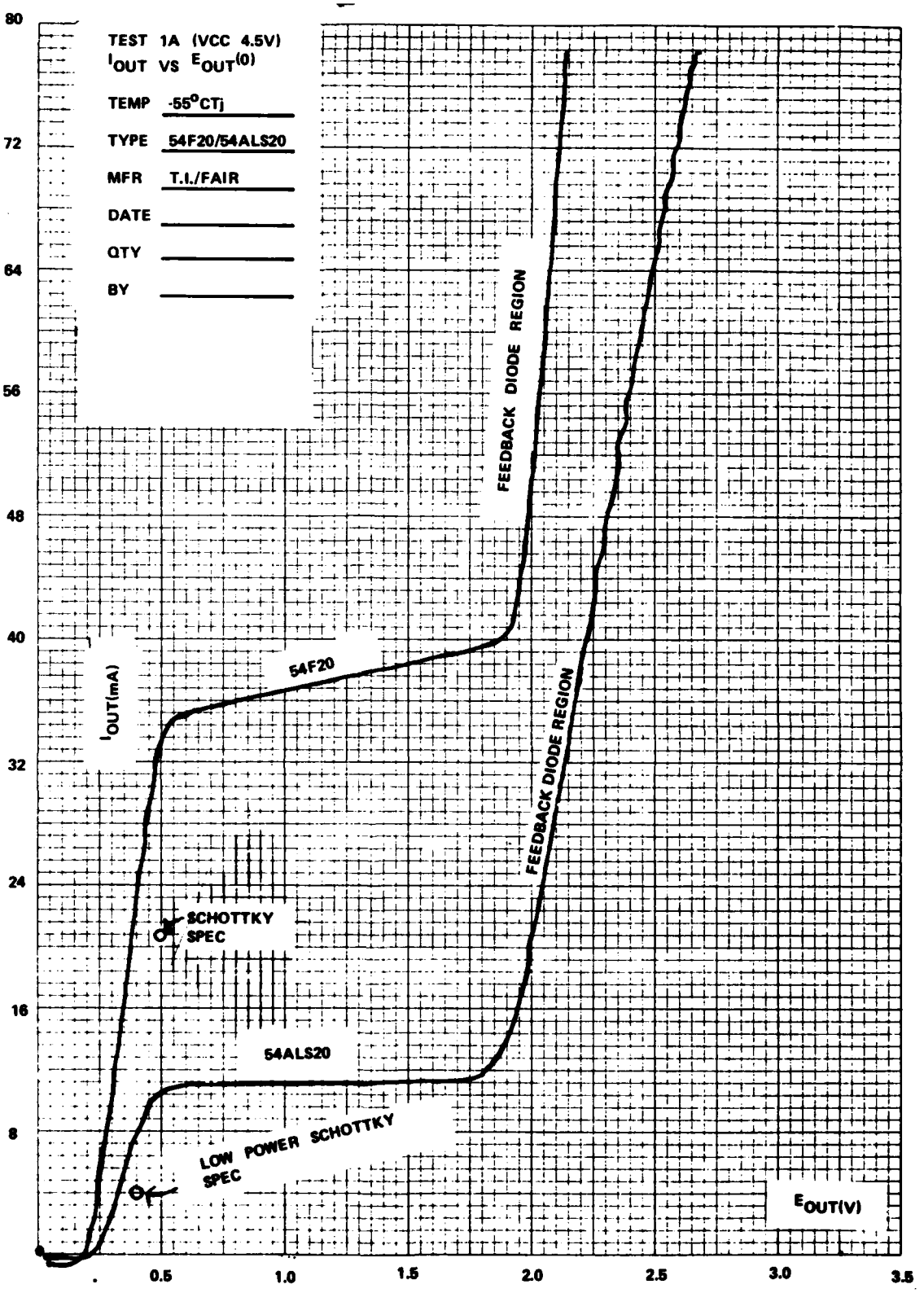


Figure 1-9. Low Power Super Schottky Technology I_{OUT} VS E_{OUT} (0)

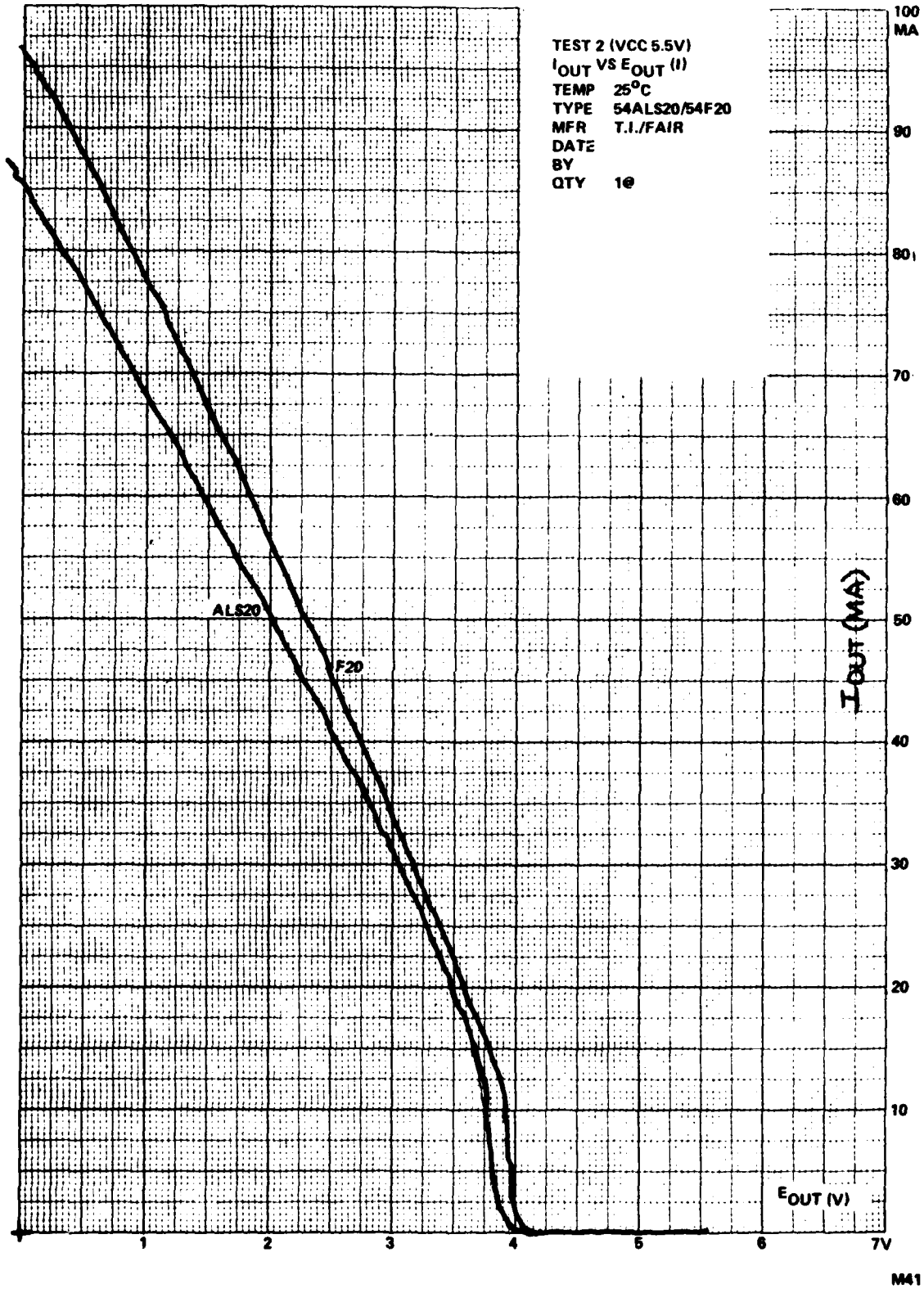


Figure 1-10. Low Power Super Schottky - I_{OUT} VS E_{OUT} (1)

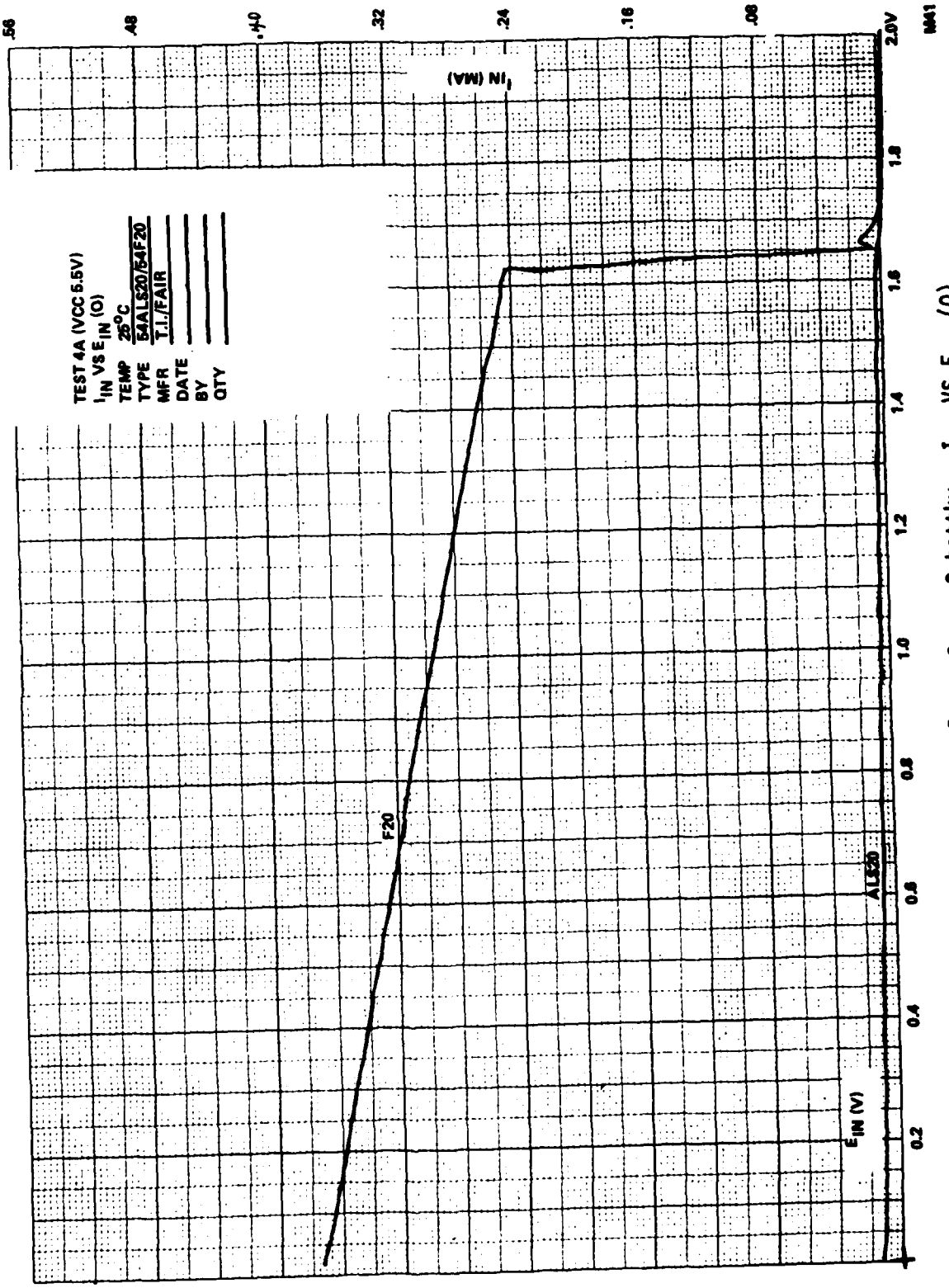


Figure 1-11. Low Power Super Schottky - I_{IN} VS E_{IN} (0)

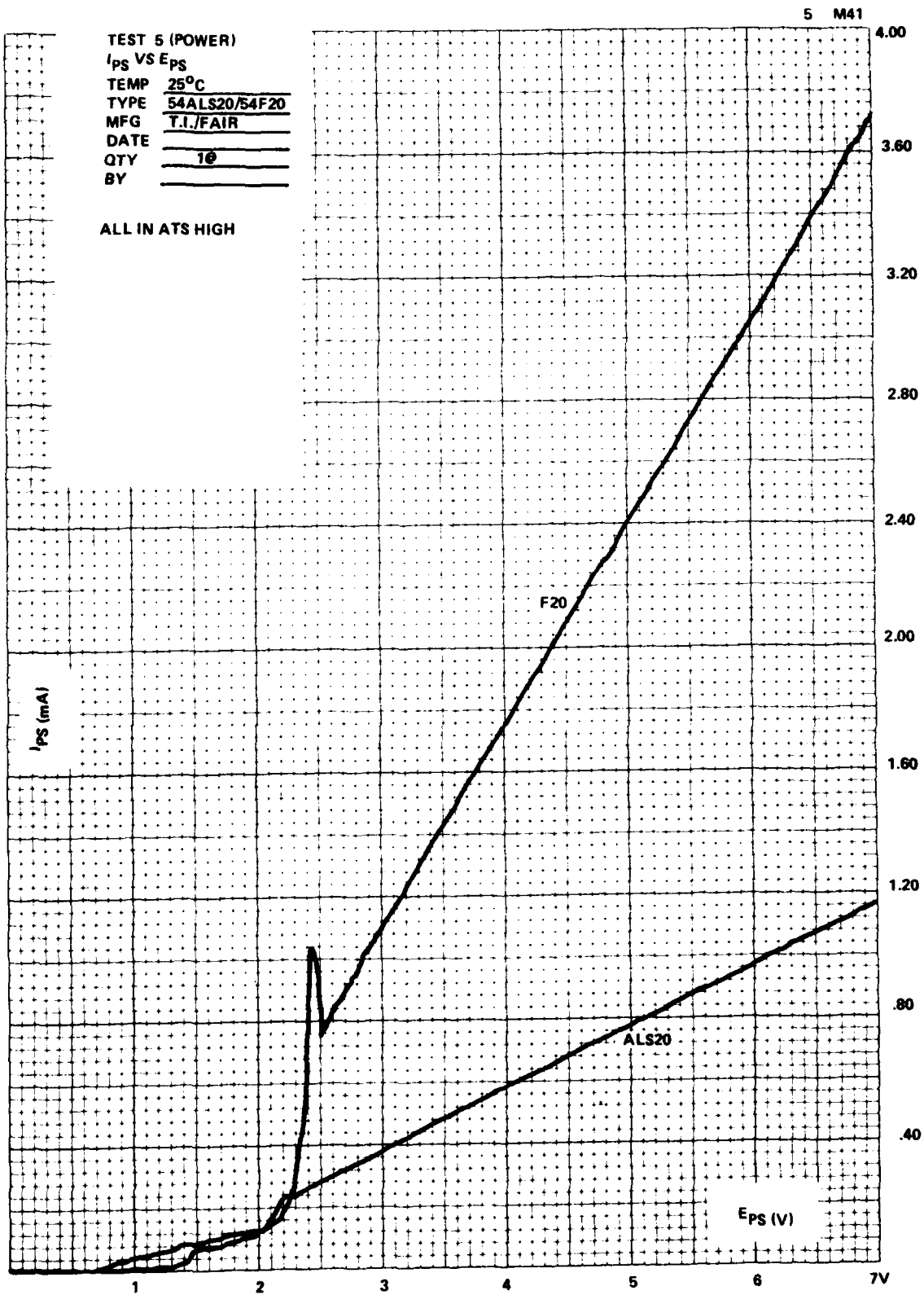


Figure 1-12. Low Power Super Schottky - I_{PS} VS E_{PS}

Table 1-2. Processing Features vs Technology

Process Feature	T.I. ALS	Fairchild FAST	T.I. AS
Ion Implantation	YES	YES	YES
Oxide-Isolation	YES	YES	YES
Walled Collectors	YES	YES	YES
Walled Bases	YES	YES	YES
Walled Emitters	NO	YES	NO
2-Layer Metal	YES	YES	YES

Section 2
SELECTION OF SAMPLES

2.1 ELIMINATION OF THE 54SSXX PRODUCT LINE

Under the Super Schottky Family, the 54SSXX series from Fairchild was proposed as a candidate for investigation, particularly because Fairchild was the only 54SSXX series vendor that employed an oxide-isolation process. Two (2) factors, however, dictated that this product line be dropped from consideration as a next generation technology: (1) Fairchild offered only 13 part types (all of which were gate and AOI functions). To obtain flip-flop samples from Fairchild would have incurred design and development costs. (2) All three vendors decided not to market the 54SSXX family. Motorola and Fairchild, however, continue to supply Super Schottky circuits for the NATO-E3A program. IBM therefore recommended that only one Super Schottky representative be analyzed, the Advanced Schottky (54ASXX) series from Texas Instruments. This recommendation was approved by RADC.

2.2 SAMPLE SELECTION AND CONSIDERATIONS

The twelve (12) part types examined under this contract are listed in Table 2-1. Four part types representing gate and flip-flop functions from each Super Schottky and Low Power Super Schottky family were evaluated. In the case of the 54ASXX family, flip-flop samples were not available within the contracted time to allow electrical evaluation. Available functions of comparable complexity were therefore suggested by IBM and approved by RADC. The high complexity functions selected were the 54AS181 and 54AS882.

Another consideration in selecting samples was to try and obtain similar, if not pin-for-pin, compatible, logic functions. For this reason the 54F181 was selected with RADC approval so that a like-function, technology comparison could be made between FAST and AS.

Table 2-1. Selected Part Types

Technology	Part Type	Vendor	Description
Super Schottky	54AS804	TI	Hex NAND Buffers
	54AS808		Hex AND Buffers
	54AS882		8-Bit Look Ahead Carry Generator
	54AS181		4-Bit Arithmetic Logic Unit (ALU)
Low Power Super Schottky	54ALS11	TI	Triple 3-Input AND
	54F11	Fairchild	Triple 3-Input AND
	54ALS20	TI	Dual 4-Input NAND
	54F20	Fairchild	Dual 4-Input NAND
	54ALS74	TI	Dual D-Flip-Flop
	54F181*	Fairchild	4-Bit ALU
	54ALS574	TI	8-Bit Flip-Flop
	54F374	Fairchild	8-Bit Flip-Flop

*The 54F175 was originally proposed but experienced late delivery.

Because of the time period during which this contract took place, the statement of work criteria that two vendors of each technology be examined, could not be met because 2nd sources for each technology did not exist.

Section 3
ELECTRICAL CHARACTERIZATION PROCEDURES AND TEST RECOMMENDATIONS

3.1 DC TEST PROCEDURES

DC tests were performed on an IBM-built tester which can test any IC package up to 40 pins in any logic family. The DC tester has the capability of conditioning a logic gate so that any input or output characteristic may be observed. These characteristics were plotted on a Hewlett-Packard X-Y recorder which provides high resolution of input and output characteristics. The DC tester was used in conjunction with a Delta 2300 temperature chamber which enabled testing over the military temperature range. Tests performed on the DC tester included I_{out} vs E_{out}, I_{in} vs E_{in}, E_{in} vs E_{out}, I_{ps} vs E_{ps}, Input Breakdown, BI_{in}, and Input Diode Clamping Voltage, V_{clamp}.

3.2 TEMPERATURE SYSTEMS

The temperature systems used by IBM to force the desired junction temperatures of the devices characterized included a Temptronix Model TP27 thermospot, and a Delta 2300 temperature chamber. All systems were accurately controlled for precision temperature testing through the military temperature range. Junction temperatures were typically forced to -55°C and 125°C.

The K-factor bar method was used by IBM to control the temperature systems in setting the desired junction temperature for devices being characterized. A K-factor bar is a silicon chip containing isolated transistor emitter-base diodes and resistors. These chips are packaged in the same type packages (14, 16, 24 pin flatpack and CDIPS) using the same die attach and bonding as is used in packaging the device to be characterized. Basically the emitter-base diodes act as thermometers. The forward voltage was measured at a constant low forward current as a function of the package ambient temperature. Since there is essentially no device power being dissipated the ambient temperature of the device packages is a close approximation of V_{BE} junction temperature. A plot of V_{BE} forward voltage vs V_{BE} junction temperature thus derived was used to determine the control setting

of a temperature forcing system to achieve any desired junction temperature. Power was dissipated in the K-factor bar equal to that of the device to be characterized. The temperature forcing system's controls were set to give the V_{BE} corresponding to the desired junction temperature. This control setting was then used to force the junctions of the devices being characterized to this same temperature as indicated by the K-factor diodes.

3.3 AC TEST PROCEDURES

IBM FSD's Electrical Characterization Laboratory maintains two independent test stations, the Tektronix model 3110 and model 3111 test systems. (See Figure 3-1). These logic testers provided for the automatic programming and data logging of most of the dynamic electrical tests performed in this study. Each test station allowed for manual and variable control of important forcing conditions such as ramp rate, DC offset, amplitude, and power supply voltages. Circuit propagation delays, output signal rise and fall rates, and output signal amplitude and offset were some of the essential AC characterization parameters which were measured directly by each system. The essential components that compromised a single Tektronix test station are described below;

1. A fast, accurate, sampling oscilloscope (Tektronix model R568) and a model R230 Digital Unit made up the heart of each station. The R568 used a model 3T6, digitally delayable, sampling time base, which had a sweep rate accuracy of $\pm$3%. The sampling rate could be set at either 100 or 1000 samples per sweep. Repeatability was better than 0.2 ns. (Refer to Table 3-1 for a chart of the 568 oscilloscope accuracy.) The R230 Digital Unit allowed for manual as well as automatic control of tester measurements, which was useful when investigating circuit aberrations or for experimentation.

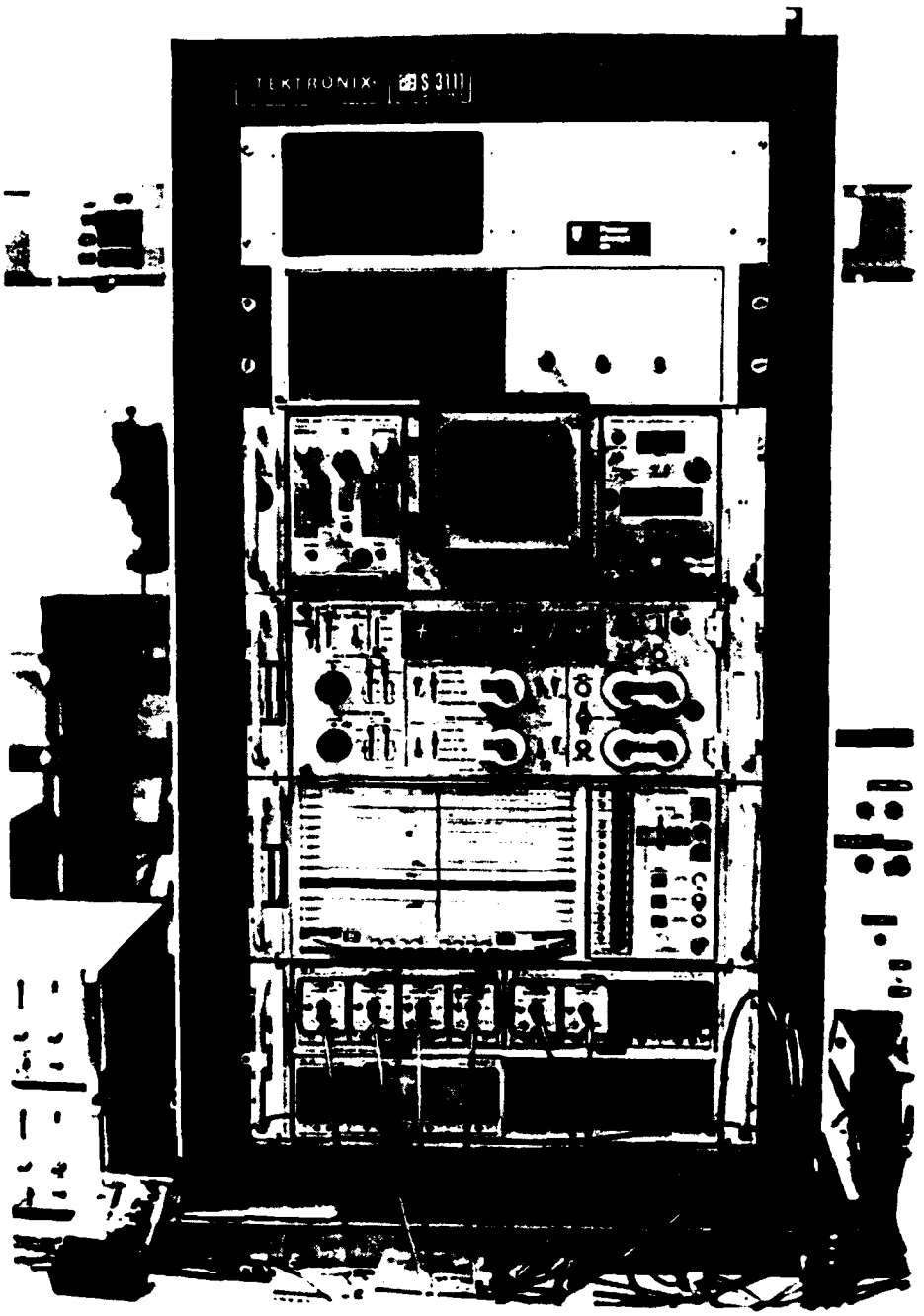


Figure 3-1. AC Characterization Test Station (1 of 2 Stations)

Table 3-1. Tektronix 3110/3111 System Accuracy

3T6 Time Base

o	Programmable Sweep Rate	- 100 ps/div to 500 ms/div in 30 calibrated steps, 1-2-5 Sequence
		- Accuracy is within 3% from 100 ps/div to 500 ps/div
o	Programmable Sampling Rate	- 100 or 1000 samples/sweep
o	Programmable Delay Range	- 0-999.9 µs Program selectable by 16-bit BCD Code in various increments

3S6 Dual Trace Sampling Units

o	Programmable Deflection Factor	- 2 mV/div to 200 mV/div in 7 calibrated steps, 1-2-5 Sequence - 3% accuracy at each step
o	DC Offset Range	- +1 V to 1 V in 5 mV Steps with 2% accuracy
o	B-Delay Range	- Channel B display can be delayed from +5 ns to -5 ns

2. The Tektronix model R241 Programmer provided the capability to implement automatic tester control. The R241 contains 14 diode matrix cards which sequentially programmed the 568 oscilloscope and the R230 Digital Unit, to perform up to 14 distinct AC parameter measurements. Devices which required more than 14 AC tests necessitated reprogramming the R241 diode matrix cards for the additional measurements.

3. High impedance sampling heads (Tektronix S-3A type) with input impedance of 100 kΩ/2.3 pF, were used for signal detection. The S-3A sampling heads have a 1 GHz bandwidth frequency response, with rise time specified at 350 ps. To eliminate long cables and maintain signal integrity, the sampling head probes monitored signals directly at the device pins. Before characterization testing, each sampling head was calibrated for DC offset, and nulled for delay differences among/between heads.

4. The electrical timing sequence for a characterization test program was controlled by a Hewlett-Packard model HP8016A Programmable Word Generator. The 8016A Word Generator provided the timing triggers to HP8082A pulse generators which developed the forcing functions to the device under test. Each pulse generator was manually adjustable in delay and ramp rate. The 8082As provided rise and fall times <1 ns/V which were necessary to properly simulate the rise and fall times of the device under test.

3.4 DEVICE TEST CONDITIONS AND RECOMMENDATIONS

Figure 3-2 illustrates the input forcing conditions used to measure the dynamic parameters of each technology tested. The timing diagram is a general one and takes into account 3-stated, high-impedance-output part types as well as timing conditions for active low-impedance output devices.

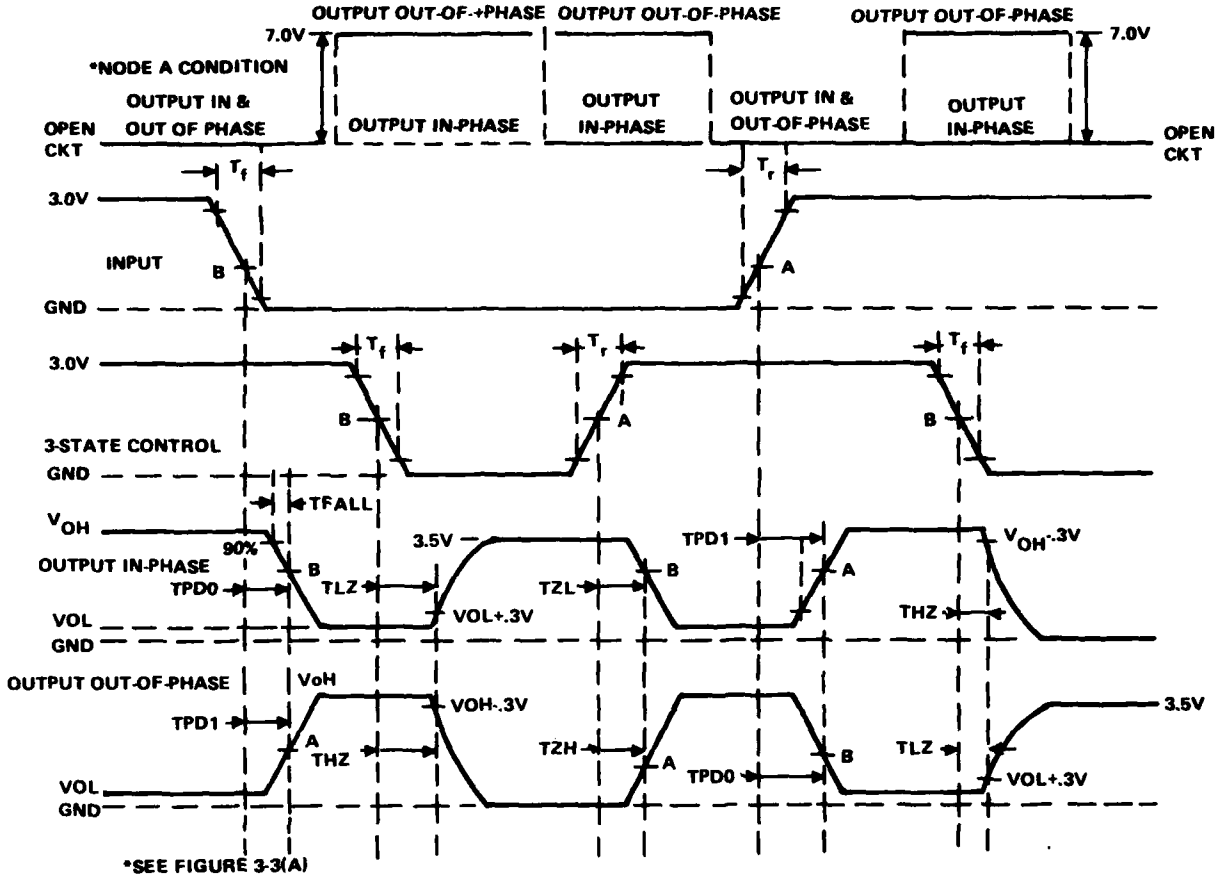
In depth AC threshold analyses were performed over the military temperature range on devices from each family. The results, as indicated in the Input Condition Table in Figure 3-2 showed AS and ALS to possess a rising and falling threshold of 1.3 volts across the military temperature range; the FAST family approximated a rising and falling threshold of 1.5 volts across temperature. These threshold analyses were in agreement with the vendor recommended thresholds for each family. Output rise and fall times were also measured for each family and based on these measurements, the input forcing function ramp rates shown in the Input Condition Table in Figure 3-2 were used for testing. ALS input rise and fall times (T_r and T_f) were set at 6.0 ns (or 2.5 ns/volt) from 0.3 V to 2.7 V on a 3.0 V amplitude pulse. Likewise, AS and FAST input T_r and T_f were set to 2.5 ns (or 1 ns/volt) from 0.3 V to 2.7 V on a 3.0 V amplitude pulse.

The set up and measurement points detailed in Figure 3-2 were used for AC test measurements on all part types tested, the results of which are detailed in Section 4 of this report. IBM recommends that the measurement points and input conditions in Figure 3-2 be used for future MIL-M-38510 specifications. TI and Fairchild have adopted this methodology.

3.5 RECOMMENDED LOAD CIRCUITS

Figure 3-3 illustrates 3 universal load configurations recommended by IBM for use in testing 3 types of device output structures, (Low-impedance bi-state totem pole output, high-impedance 3-state output, and open collector output) of all new TTL bipolar logic families. These circuits have several advantages over the 3 traditional load circuits employed by most IC manufacturers (see Figure 3-4). The advantages are discussed below:

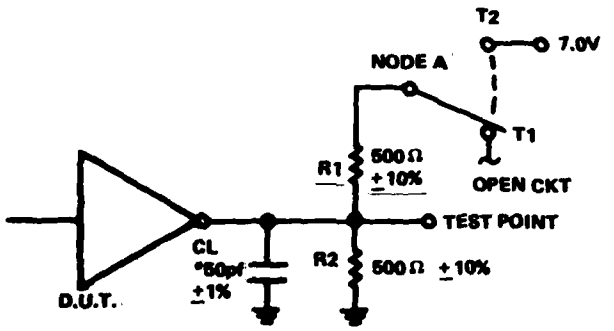
1. The load circuits in Figure 3-3(A) and 3-3(C) simplify the building of test fixtures when compared to the separate bi-state and 3-state load circuits in Figure 3-4(A) and 3-4(C). Open collector output measurements can also be done with circuit, Figure 3-3(A), if the output is capable of sinking 12 mA. Therefore, essentially Figure



INPUT CONDITION TABLE

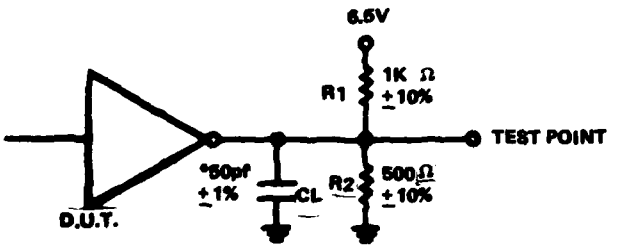
FAMILY	INPUTS T_r (ns)	INPUTS T_f (ns)	THRES-HOLD	JUNCTION TEMPERATURES °C -55V	+25V	+125V
ALS	6.0	6.0	A	1.3V	1.3 V	1.3 V
			B	1.3V	1.3 V	1.3 V
AS	2.5	2.5	A	1.3 V	1.3V	1.3 V
			B	1.3 V	1.3 V	1.3 V
FAST	2.5	2.5	A	1.5 V	1.5 V	1.5 V
			B	1.5 V	1.5 V	1.5 V

Figure 3-2. Input Conditions and Measurement Definitions

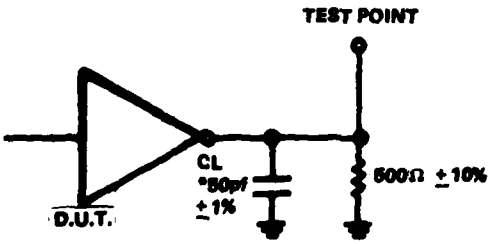


PARA-METER	NODE A SWITCH POSITION			
	3-STATE OUTPUT		OPEN COLLECTOR OUTPUT	
	T1	T2	T1	T2
TPD1	CLOSED	OPEN	OPEN	CLOSED
TPD0	CLOSED	OPEN	OPEN	CLOSED
THZ	CLOSED	OPEN	N/A	N/A
TZH	CLOSED	OPEN		
TL2	OPEN	CLOSED		
TZL	OPEN	CLOSED		

(A) LOAD CKT FOR 3-STATE OUTPUTS; OPEN COLLECTOR OUTPUTS (IOL>12mA)
RECOMMENDED FOR: FAST, AS AND ALS.



(B) LOAD CKT FOR OPEN COLLECTOR OUTPUT (IOL<12mA)
RECOMMENDED FOR: ALS.



(C) OPTIONAL LOAD CKT FOR BI-STATE OUTPUTS RECOMMENDED
FOR: FAST, AS AND ALS.

*CL-REPRESENTS THE TOTAL OF LOAD CAPACITANCE AND FIXTURE CAPACITANCE.

Figure 3-3. Universal Load Circuits Recommended for Future MIL-M-38510

3-3(A) can be used to test bi-state, 3-state, and open collector circuits, which traditionally would have required the 3 separate load circuits in Figure 3-4.

2. The load circuit in Figure 3-3(B) is recommended for testing open collector ALS circuits which have low output sinking capability. It requires an additional 500 Ω resistor to ground (not used in traditional circuit in Figure 3-4(B)) but this is used to establish and standardize a testing output up level of 2.2 volts.

3. The timing diagram and measurement points detailed in Figure 3-2, are standardized and established by the load circuits in Figure 3-3. Tri-State delays such as TLZ and THZ are established by the load circuit of Figure 3-3(A) and the measurement points defined in Figure 3-2. TLZ and THZ measurements are taken at 0.3 V above the output down level and 0.3 V below the output up-level respectively. Open collector delays will also be standarized with the newly recommended circuits. Open collector measurements are taken to the circuit threshold.

4. Node A (see Figure 3-3(A)) can be switched by a programmable supply, pulse generator, driver, or relay, thereby allowing direct sequential programming of delay measurements without stopping test to manually switch Node A or change test fixture. When driven by a power supply, driver, or pulse generator (when open ckt cannot be switched) a silicon switching diode should be placed in series with R1 and the voltage at Node A raised according to the forward voltage drop of the diode chosen (see Figure 3-6).

5. The value of R2, 500 Ω is chosen specifically to allow the use of low impedance 50 Ω test probes as well as high impedance sampling probes or FET probes. On a low impedance 50 Ω test system, the 500 Ω pull-down resistor can be represented by a 450 Ω resistor in a series with the input impedance of the test probe to ground, creating a 10 to 1 divider. This test set-up is illustrated in Figure 3-5 below.

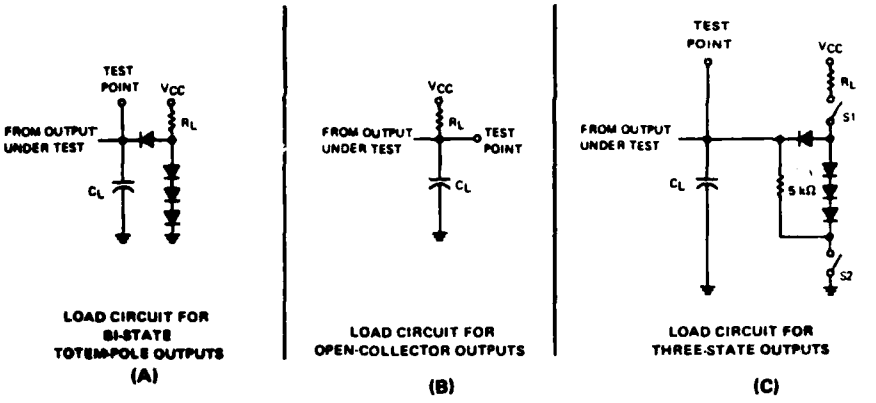


Figure 3-4. Traditional Load Circuits Employed by Most IC Manufacturers

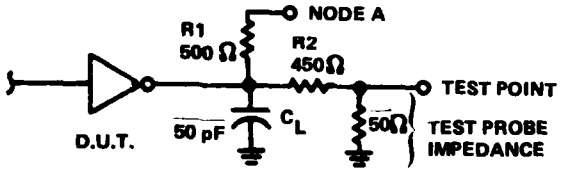


Figure 3-5. Low Impedance 50 Ohm Test System Showing Load Modification

In this study all bi-state devices were tested with the optional load circuit in Figure 3-3(C). A 510 Ω ±10% carbon resistor and a 47 pF ± 1% chip capacitor (Vitramon part no. EJ-0805A-470-FF) were used.

Tri-state devices were tested with the load circuit of Figure 3-3(C), with a slight modification. A silicon switching diode (1N4148) having a forward voltage drop of ≈.7 volts was placed in series with R1, with the anode connected to Node A and the cathode to R1. (see Figure 3-6). Node A was conditioned with an unterminated 8082A pulse generator, which switched

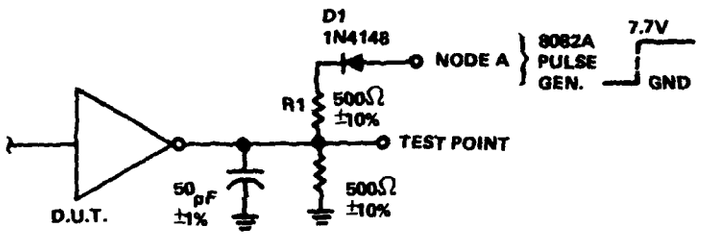


Figure 3-6. Modified Universal Load Circuit Used by IBM to Test 3-State Devices

between GND and 7.7 volts. Grounding Node A reverse biases D1 which effectively removes R1 from the load circuit for bi-state, THZ and TZH delay measurements. (Refer to the timing diagram in Figure 3-2.)

The open collector output of the 54F181 was tested with the load circuit in Figure 3-3(C), but with a 500 Ω pull-up to V_{CC}.

Section 4
CHARACTERIZATION RESULTS AND TECHNOLOGY COMPARISONS

In this section room temperature AC characterization results are summarized and presented for each family and part type tested. Summarized data over the military temperature range and at three power supply voltages (4.5 V, 5.0 V, and 5.5 V) are available for each part type in Appendix A. DC characteristics over temperature for each part type are also available in Appendix B.

4.1 TI's ADVANCED SCHOTTKY (54ASXX) FAMILY

In the Advanced Schottky (AS) Family the following four part types were characterized; 54AS804, 54AS808, 54AS181, and 54AS882.

4.1.1 54AS804

The 54AS804 is a Hex 2-Input NAND Buffer gate in a 20 pin package. A logic diagram of the 54AS804 is depicted in Figure 4-1. The average room temperature ambient performance observed on this part type is detailed in Table 4-1. Twenty-five (25) samples were tested at 25°C T_A, and 15 samples at -55°CT_J and +125°CT_J. The performance of a 54S04 is included in Table 4-1. Although this comparison is not a valid one because of the high drive capability of the 54AS804 over the 54S04, it does offer an indication of the performance achieved by a typical AS gate with respect to that of a Schottky gate.

Table 4-1. 5.0 V, 50 pF, 25°C Average Performance/Power
54AS804 vs 54S04

Delay Path	54AS804	54S04
A - Y TPD1	2.9 ns	3.9 ns
A - Y TPD0	3.2 ns	5.8 ns
5.0 V DC Power/Pkg.	120 mW	128 mW

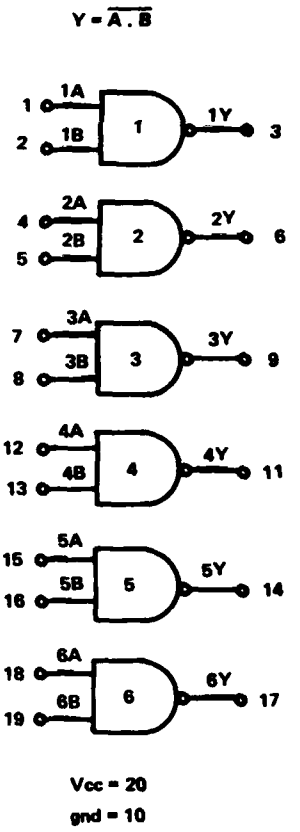


Figure 4-1. Functional Logic Diagram of the 54AS804

The average delay of the AS804 was 35% faster than that of the 54S04. The 54AS804 dissipated 6% less power than the 54S04. It exhibited excessive high temperature slowdown between room temperature and +125°C T_j, averaging 45% on TPD1's @ 50 pF. (Refer to Appendix A pages 1, 2 and 3.) Excessive input leakage current was also observed @ +125°C T_j, averaging 200 µA @ 1.5 volts V_{IN}. (See I_{IN} vs E_{IN} plot on page 4, Appendix B.) Input leakage should not exceed 100 µA @ 7.0 volts. The I_{OL} observed at V_{OL} = 0.5 V, -55°C T_j, 4.5 V V_{cc} was 55 mA. (See Appendix B page 1.)

4.1.2 54AS808

The 54AS808 is a Hex 2-Input AND Buffer gate in a 20 pin package. A logic diagram of the 54AS808 is shown in Figure 4-2. Like the 54AS804, the 54AS808 has a higher drive characteristic than the 54S08. The comparison therefore in Table 4-2 is not one-to-one, but does offer an assessment as to the degree of speed enhancement of the 54AS808. The 54S08 is a quad 2 input AND gate, and therefore a per gate rather than a per package power comparison is made. Twenty-five samples were tested at 25°C T_A, and 16 samples at both -55°C T_j and +125°C T_j.

Table 4-2. Average 5.0V, 25°C, 50 pF Performance/Power
54A808 vs 54S08

Delay Path	54AS808	54S08
A - Y TPD1	4.1 ns	5.9 ns
A - Y TPD0	4.4 ns	6.7 ns
5.0 V D.C. Power/Gate	24.2 mW	31.3 mW

The 54AS808 showed an average 32% improvement in speed over the similar Schottky gate function. It also dissipated 23% less power than the 54S08. This part experienced the same type of +125°C T_j input leakage problem

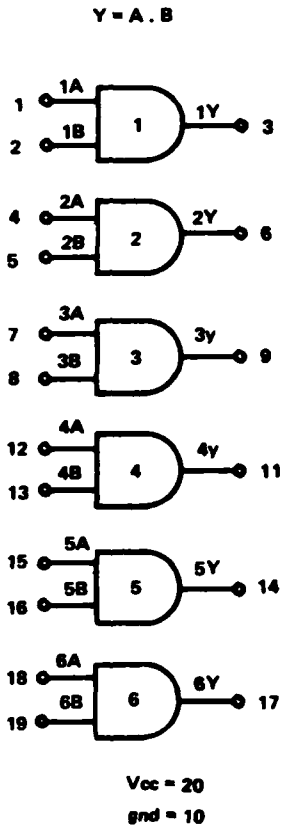


Figure 4-2. Functional Logic Diagram of the 54AS808

observed on the 54AS804. An input leakage current of 0.6 mA @ 2.2 volts was measured. (See Appendix B, page 9.) A 42% high temperature slow down was observed in TPD1 delays. The IOL observed at V_{OL} = 0.5 V, -55°C T_j, 4.5 V V_{CC} was 35 mA (see Appendix B, page 6). Appendix A, pages 4, 5 and 6, contain the average, maximum, and minimum AC parameters measured over the military temperature range and $\pm$10% V_{CC} on the 54AS808. Appendix B, pages 6 thru 10, contains the DC characterstics.

4.1.3 54AS181 AND 54F181

Because of the equivalency of function, results from both the AS and FAST functions are presented here. The 54AS181 and 54F181 are 4-bit Arithmetic Logic Units (ALU) designed in 24 pin packages. Figure 4-3 shows a logic diagram of these devices. Both devices are pin-for-pin compatible and functionally equivalent to the 54S181, Schottky part type.

Seven distinct circuit delay paths were tested in the SUM Mode of operation, and these measurements, along with equivalent Schottky delays are compared in Table 4-3.

Twenty-eight (28) samples of each family were tested at 25°C, and 10 samples of each family at -55°C T_j and +125°C T_j.

The data in Table 4-3 shows that the 54F181 was faster than the 54AS181 in eleven (11) out of the fourteen (14) Sum Mode delays. Over the eleven (11) delays, the 54F181 ranged from 0.3 ns to 3.6 ns faster, for an average of about 1.2 ns faster. Over the three Sum Mode delays for which the 54F181 was slower than the 54AS181, the average was 0.4 ns. The 54F181 dissipated approximately 2/3 less power than the 54AS181. Sum Mode AC data for the 54AS181 can be found on pages 7 thru 9 of Appendix A, while data for the 54F181 are on pages 10 thru 12 of Appendix A. No abnormal DC characteristics such as input leakage were observed on either part. The 54AS181 had an I_{OL} of 32 mA @ V_{OL} = 0.5 V, -55°CTj, while the 54F181 averaged 26 mA

functional block diagram

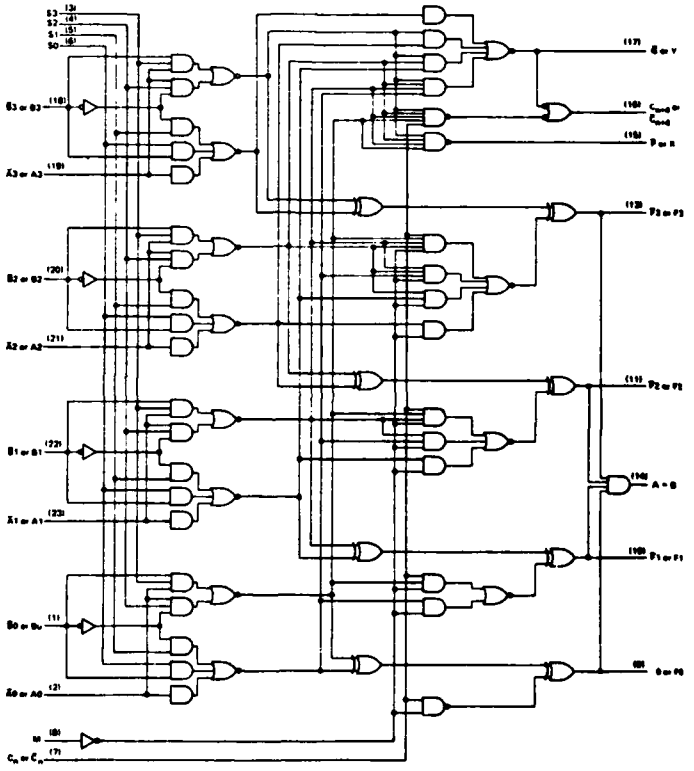


Figure 4-3. Functional Logic Diagram of the 54AS181 and 54F181

Table 4-3. 5.0 V, 25°C, 50 pF
Average SUM Mode Performance/Power
54AS181 vs 54F181 vs 54S181

	Delay Path	54AS181	54F181	54S181
1)	B0 - F0 TPD1 (IP)	6.7 ns	7.2 ns	11.9 ns
	TPD0 (OP)	10.8 ns	7.2 ns	14.0 ns
2)	B0 - F3 TPD1 (OP)	7.6 ns	7.8 ns	14.0 ns
	TPD0 (OP)	8.7 ns	7.1 ns	14.0 ns
3)	B0 - P TPD1 (IP)	5.3 ns	4.9 ns	8.9 ns
	TPD0 (IP)	6.9 ns	5.4 ns	8.5 ns
4)	B1 - G TPD1 (IP)	6.5 ns	5.6 ns	9.2 ns
	TPD0 (IP)	6.0 ns	5.1 ns	7.4 ns
5)	B1 - CN+4 TPD1 (OP)	9.8 ns	9.5 ns	11.9 ns
	TPD0 (OP)	9.2 ns	8.9 ns	14.5 ns
6)	CN - F3 TPD1 (IP)	5.4 ns	5.8 ns	8.3 ns
	TPD0 (IP)	6.5 ns	5.3 ns	9.4 ns
7)	CN - CN+4 TPD1 (IP)	6.5 ns	5.2 ns	8.2 ns
	TPD0 (IP)	5.5 ns	4.9 ns	9.0 ns
5.0 V DC Power		490 mW	170 mW	560 mW

I_{OL} @ V_{OL} = 0.5 V, -55°CTj. (See I_{OUT} v.s. E_{OUT} (0) plots of each family on pages 11 and 20 of Appendix B). In the Sum Mode the 54AS181 slowed down from room to +125°CTj an average of 27% while the 54F181 slowed down an average of 12%.

In comparing the FAST and AS ALU to the Schottky ALU it can be seen that the 54AS181 outperforms the 54S181 by an average of 31% on all Sum Mode paths with a 13% reduction in power; the FAST ALU averages 39% better performance than the Schottky ALU, with a 70% reduction in power.

Table 4-4 compares the Difference Mode performance observed on the three ALU. Six worst-case circuit paths were tested in the Difference Mode. Data on some paths of the 54S181 were not available.

Table 4-4. 5.0 V, 25°, 50 pF
Average Difference Mode Performance
54AS181 vs 54F181 vs 54S181

	Delay Path		54AS181	54F181	54S181
1)	B0-F0	TPD1 (IP)	8.9 ns	7.4 ns	15.8 ns
		TPD0 (OP)	12.3 ns	7.9 ns	N/A*
2)	B0-P	TPD1 (OP)	7.1 ns	5.7 ns	9.8 ns
		TPD0 (OP)	7.6 ns	6.4 ns	11.8 ns
3)	B1-G	TPD1 (OP)	8.2 ns	6.5 ns	N/A
		TPD0 (OP)	6.4 ns	6.3 ns	N/A
4)	B1-CN+4	TPD1 (IP)	10.5 ns	10.6 ns	15.3 ns
		TPD0 (IP)	10.9 ns	9.8 ns	16.0 ns
5)	B0-A=B	TPD1 (OP)	25.9 ns	29.3 ns	N/A
		TPD0 (IP)	12.8 ns	9.3 ns	N/A
6)	M-F_3	TPD1 (OP)	7.5 ns	7.4 ns	N/A
		TPD0 (OP)	7.2 ns	6.4 ns	N/A

* N/A - Not Available

The above data shows that the 54F181 outperforms the 54AS181 in ten (10) out of the twelve (12) Difference Mode delays. Over the ten (10) delays the FAST 181 ranged from 0.1 ns to 4.4 ns faster than the AS181 for an average of 1.6 ns faster. The 54F181 was slower than the 54AS181 by 0.1 ns in the B1-CN+4 TPD1 delay and by 3.4 ns in the B0-A=B TPD1 delay (which has an open collector output). A load capacitance of 50 pF, a 500 Ω pull-down resistor and a 500 Ω pull-up resistor to V_{CC} was used as a load on this open collector output. This accounts for an RC time constant of approximately 12.5 ns. The 54F181 TPD1 was measured to 1.5 volts while the 54AS181 TPD1 was measured to 1.3 volts. This 0.2 volt difference in measurement point can account for a

2.7 ns difference in delay based on the RC time constant. A comparable 54F181 B0-A=B TPD1 delay should therefore read ≈26.6 ns if measured to 1.3 volts.

High temperature slowdown in the Difference Mode was more pronounced than in the Sum Mode on the 54AS181, averaging 32%. The 54F181 averaged 19%. For five of the Difference Mode delays in Table 4-4, data for the Schottky ALU is provided. The 54AS181 averages 34% speed improvement over the 54S181, while the FAST 181 averaged 42% speed enhancement.

The 54AS181 was a first iteration design, while the 54F181 represented a third iteration design. TI is expected to redesign and make process adjustments to this part. Performance improvement is therefore expected with maturity of the AS line.

4.1.4 54AS882

The 54AS882 is a 32-bit Look-Ahead Carry Generator designed in a 24 pin package. It is intended to take the place of two 54S182's. A logic diagram of the 54AS882 is shown in Figure 4-4. Eighteen (18) samples were tested at 25°C T_A and 10 samples at -55°C T_j and +125°C T_j. Table 10 summarizes the average room temperature performance measured on six different delay paths.

The 54AS882 achieves approximately 38% speed improvement over the 54S182 on the single comparable path CN-CN+8 shown in Table 4-5. What is significant to note is that the Schottky power dissipation has been maintained while doubling the circuit complexity. The 54AS882 had abnormally low current gain, h_{fe}, in its output transistors as the I_{out} VS E_{out} (0) plot on page 27, Appendix B indicates. The devices are just meeting the Schottky specification of 20 mA @ 0.5 V, -55°C T_j and sink current at 1.5 volts, V_{OL} is less than 30 mA over the 10 samples tested. An I_{OL} characteristic similar to the 54AS181 would have been expected since these two part types both have standard AS output structures.

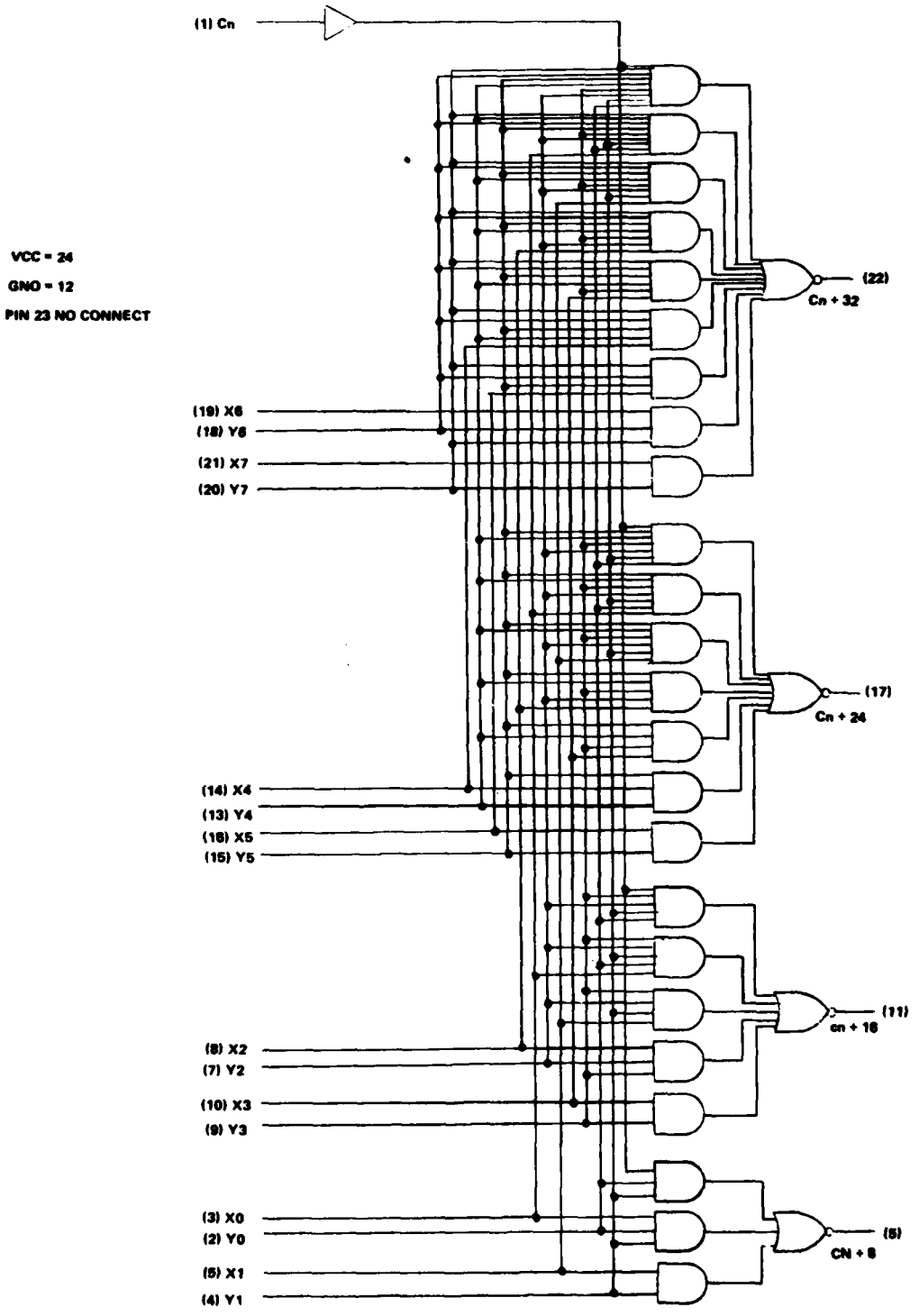


Figure 4-4. Functional Logic Diagram of the 54AS882

Table 4-5. 5.0 V, 25°C, 50 pF
Average Performance/Power
54AS882

Delay Path	54AS882	54S182
Y3 - CN+32 TPD1	4.7 ns	-
Y3 - CN+32 TDP0	5.4 ns	-
X6 - CN+32 TDP1	3.9 ns	-
X6 - CN+32 TPD0	4.0 ns	-
X0 - CN+8 TPD1	3.2 ns	-
X0 - CN+8 TPD0	4.6 ns	-
CN - CN+32 TPD1	6.5 ns	-
CN - CN+32 TPD0	7.8 ns	-
CN - CN+24 TPD1	6.1 ns	-
CN - CN+24 TPD0	6.9 ns	-
CN - CN+8 TPD1	4.6 ns	7.6 ns
CN - CN+8 TPD0	6.5 ns	10.2 ns
5.0 V DC Power/Pkg	240 mW	240 mW

Examination of the I_{out} vs E_{out} (0) characteristic of the 54AS882 on page 27 of Appendix B, indicates that the forward drop on the output feedback diode is abnormally high especially at -55°C T_j, where the knee of the feedback diode region is around 2.25 volts. This knee should normally occur between 1.8 and 2.1 volts. This implies that the forward resistance of the feedback diode is high which denies base drive to the output transistor. This is evident in the flatter slope of the feedback diode region. All parts would have problems providing reflected wave switching in a low impedance 30 ohms transmission line environment.

The overall performance achieved by the 54AS882 is impressive and would provide valuable system enhancement as well as space savings.

4.2 FAIRCHILD'S ADVANCED SCHOTTKY TTL (54FXXX) FAMILY

The following four part types in addition to the 54F181 discussed above were characterized; 54F11, 54F20, 54F175 and 54F374.

4.2.1 54F11

The 54F11 is a Triple-3-Input AND gate in a 14 pin package. A logic diagram of the device is shown in Figure 4-5. The average ambient room temperature performance and power observed on this part type is detailed in Table 4-6 and compared to the performance of the 54S11, its Schottky equivalent. Thirty (30) samples were examined at 25°C T_A and ten (10) samples at both -55°C T_j and +125°C T_j.

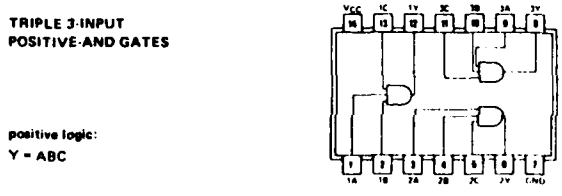


Figure 4-5. Functional Logic Diagram of the 54F11

Table 4-6. 5.0 V, 25°C, 50 pF
Average Performance/Power
54F11 vs 54S11

Delay Path	54F11	54S11
A-Y TPD1	4.7 ns	5.2 ns
A-Y TPD0	4.2 ns	6.6 ns
5.0 V DC Power/Pkg	24.0 mW	94.0 mW

The 54F11 averaged 10% improvement over the 54S11 on a TPD1 delay, and 36% speed improvement on a TPD0 delay. A significant power savings was realized by the 54F11, showing a 74% reduction under the Schottky part. The gains of the output transistors on the ten 54F11 devices tested were low and none of the samples met the Schottky specification of I_{OL} = 20 mA @ V_{OL} = 0.5V, -55°C T_j. The I_{out} vs E_{out} (0) plot shows this on page 32 of Appendix B (shows I_{OL} = 18 mA at V_{OL} = 0.5 V, T_j = -55°C). Two (2) devices out of the ten (10) examined showed abnormal characteristics including excessive output leakage current of 2 mA @ E_{out} = 5.0 volts (see I_{out} vs E_{out} (1) plot page 33 Appendix B) and Darlington breakdown at V_{CC} >6.0 volts. See I_{ps} vs E_{ps} on page 34 Appendix B. The I_{os} measured at 25°C T_A averaged 85 mA. The AC performance data over the military temperature range and ± 10% supply voltage of the 54F11 are available on pages 22 thru 24 of Appendix A.

4.2.2 54F20

The 54F20 is a Dual 4-Input NAND Gate in a 14 pin package. A logic diagram of this device is shown in Figure 4-6. Twenty-nine (29) samples were tested at 25°C T_A and ten (10) samples at both -55°C T_j and -125°C T_j. Table 4-7 summarizes the room temperature ambient performance of the 54F20. A comparison is made to the performance under similar load condition (50 pF) of the 54S20.

Table 4-7. 5.0 V, 25°C, 50 pF
Average Performance/Power
54F20 vs 54S20

Delay Path	54F20	54S20
A - Y TPD1	3.6 ns	3.9 ns
A - Y TPD0	2.9 ns	6.4 ns
5.0 V DC Power/Pkg	8.0 mW	40 mW

Only 8% speed improvement on a TPD1 delay was achieved by the 54F20 over the 54S20. A 55% speed improvement over the 54S20 was achieved on a TPD0 delay. The 54F20 dissipated 1/5 the power of the 54S20. It exhibited an I_{OL} of 33 mA @ V_{OL} = 0.5 V, T_j = -55°C and an I_{os} of 84 mA, @ T_j = +125°C. These characteristics can be seen on pages 38 and 39 of Appendix B. AC parameters over temperature and ±10% supply voltages are available on pages 25, 26 and 27 of Appendix A.

DUAL 4-INPUT
POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABCD}$

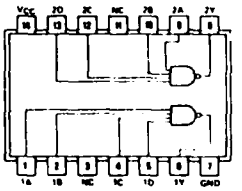


Figure 4-6. Functional Logic Diagram of the 54F20

4.2.3 54F374

The 54F374 is an Octal D-Type Flip-Flop with 3-state outputs in a 20-pin package. A logic diagram of this device appears in Figure 4-7. Thirty samples of this device were tested @ -55°C T_j, 25°C T_A, and +125°C T_j. Characterization of this part was performed before the adoption of the universal load circuit discussed in Section 3. The 54F374 was characterized at 3 capacitive loads, 50 pF, 150 pF, and 250 pF on clock to output bi-state delays. A 5 kilohm pull-down resistor was used in parallel with each lumped capacitor. Later experiments determined that there was insignificant difference in delays between the newly adopted 500 ohm/50 pF load and the 5 kilohm/50 pF load used. TZH and TZL delays of the 54F374 were taken with a 5 kilohm/50 pF load. TLZ delays were taken with a 5 kilohm resistor to V_{cc} and a 25 pF capacitor to ground as a load. THZ delays were taken with a 1 kilohm resistor to ground and a 25 pF capacitor to ground. The room temperature ambient 50 pF delays observed on this device are presented below in Table 4-8.

Delays and power for the 54S374 were estimated from vendor catalog 25°C, 5.0 V, 15 pF, data and do not represent actual measurements. They do, however, offer a technology comparison. AC performance data of the 54F374 over temperature and ±10% V_{CC} are available on pages 28 thru 30 of Appendix A. DC characteristics are presented on pages 44 thru 49 of Appendix B.

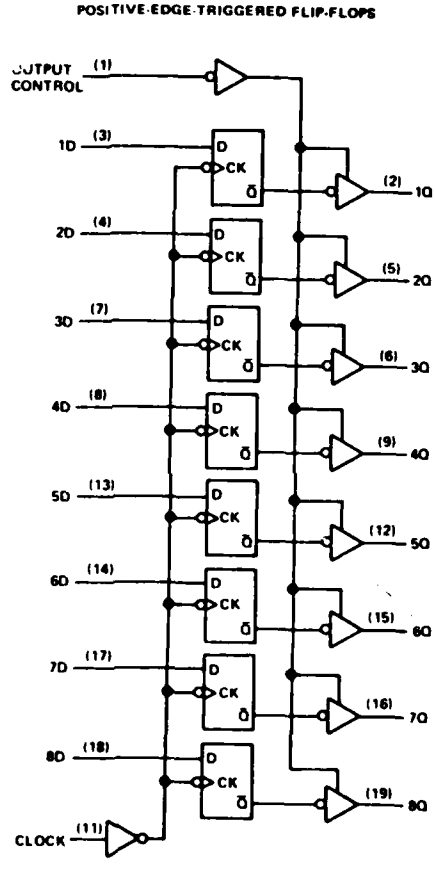


Figure 4-7. Functional Logic Diagram of the 54F374

Table 4-8. 5.0 V, 25°C, 50 pF
Average Performance/Power
54F374 vs 54S374

Delay Path	54F374	54S374
Clock - Q TPD1	5.2 ns	10.0 ns
Clock - Q TPD0	6.5 ns	14.8 ns
TLZ	7.1 ns	* N/A
THZ	4.1 ns	* N/A
TZL	5.3 ns	8.0 ns
TZH	4.5 ns	11.0 ns
5.0 V DC Power/Pkg	163 mW	450 mW

* N/A = Not Available

The 54F374 averages 47% speed improvement over the 54S374 on the Clock-Q delays shown in Table 4-8. A 64% reduction under Schottky power is estimated. The 54F374 averages 26 mA, I_{OL} @ V_{OL} = 0.5 V, T_j = -55°C and Ios = 90 mA at T_A = 25°C. (See pages 44 and 45 of Appendix B.)

The 54F374 exhibited 30% 25°C T_A to +125°C T_j slowdown on CLK-Q TPD0 delays, which implied some degree of storage on internal registers before the output buffer. This slowdown is especially evident on TLZ delays. (See page 28 Appendix A.)

Table 4-9 summarizes the average room temperature, 5.0 volt V_{cc} miscellaneous AC parameters tested on the 54F374.

Table 4-9. Miscellaneous Performance Data, 5.0 V, 25°C T_a

Parameter	Avg Data
Set '1'	+.1 ns
Set '0'	-.3 ns
Hold '1'	+.3 ns
Hold '0'	+.3 ns
Minimum Positive CLK Pulse	3.7 ns
Minimum Negative CLK Pulse	1.5 ns
Maximum CLK Frequency	130 MHz

4.2.4 54F175

The 54F175 is a Quad D-Type Flip-Flop with Clear. It is available in a 16 pin package. A logic diagram of the 54F175 is shown in Figure 4-8. Thirty (30) samples were tested at 25° C T_a, and ten (10) samples at -55°C T_j and +125°C T_j. The average room temperature performance observed on the 54F175 is presented in Table 4-10 along with that of the 54S175.

Table 4-10. 5.0 V, 25°C, 50pF AveragePerformance/Power
54F175 vs 54S175

Delay Path	54F175	54S175
CLK-Q TPD1	5.2 ns	10.0 ns
CLK-Q TPD0	6.1 ns	14.8 ns
CLK-$\overline{Q}$ TPD1	5.0 ns	10.5 ns
CLK-$\overline{Q}$ TPD0	6.3 ns	14.9 ns
CLR-Q TPD0	7.2 ns	15.9 ns
CLR-$\overline{Q}$ TPD1	6.2 ns	11.4 ns
5.0 V DC Power	110 mW	330 mW

Table 4-10 shows that the 54F175 averages 53% faster delays than the 54S175 over the six (6) delays shown, at 2/3 less power. Average AC performance data across the military temperature range and ±10% V_{CC} is available on pages 31 thru 33 of Appendix A. Appendix B - pages 50 thru 61 contains pertinent DC characteristics.

Summarized in Table 4-11 is the average room temperature, 5.0 volt miscellaneous performance parameters tested on the 54F175.

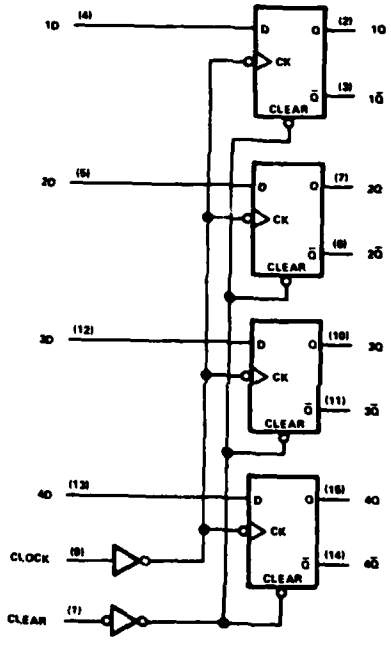


Figure 4-8. Functional Logic Diagram of the 54F175

Table 4-11. Miscellaneous Performance Data, 25°C, 5.0 V
54F175

Parameter	Data
Set '1'	+0.9 ns
Set '0'	+1.5 ns
Hold '1'	-1.1 ns
Hold '0'	-0.4 ns
Minimum Positive CLK Pulse	2.0 ns
Minimum Negative CLK Pulse	3.1 ns
Minimum CLR to CLK Enable Time	3.1 ns
Maximum Clock Frequency	166 MHz

A high V_{CC} output breakdown anomaly was discovered on the 54F175. It is evident in the I_{PS} vs E_{PS} plot on page 54 Appendix B, and occurs when the output is switched from a HIGH to a LOW state with V_{CC}>6.0 volts. Experiments showed that the output Darlington transistors have low BV_{CE} (collector-emiter breakdown) allowing breakdown to occur after a HIGH to LOW transistion. Both Darlington transistors' base-emitter junctions remain slightly forward biased when the output has switched LOW (0.2 volts) and the base of the upper Darlington transistor is sitting at $(V_{BE} + V_{SAT}) \approx 1.0$ to 1.1 V. This condition allows for a lower BV_{CE} voltage on the Darlington.

Other FAST devices examined also experienced similar breakdown but at a higher V_{CC} i.e. V_{CC}>7.0 volts. In all cases this was a recoverable condition. Fairchild was informed of this anomaly. It is IBM's opinion that this phenomena is not a critical problem, and should not be a factor under normal operating conditions. This particular lot of 54F175 Flip-Flops had a BV_{CE} lower than all other FAST parts examined. This low BV_{CE} should go higher as the process is stabilized.

4.3 TI'S ADVANCED LOW POWER SCHOTTKY (54ALSXX) FAMILY

The four part types examined in this family were; 54ALS11, 54ALS20, 54ALS74, and 54ALS574. Characterization results for each of the above part types are presented here.

4.3.1 54ALS11

The 54ALS11 is a Triple 3-Input AND gate in a 14 pin package. A logic diagram of the device is shown in Figure 4-9. The average ambient room temperature performance and power observed on this device is detailed in Table 4-12. It is compared to the performance of its Low Power Schottky (LS) equivalent function, the 54LS11, under similar load conditions. Twenty-five (25) samples were tested at 25°C T_A and ten (10) samples at -55°C T_j and +125°C T_j. All three (3) gates in the 54ALS11 package were tested. Average room temperature delays among the gates ranged from 9.7 ns to 14.5 ns on a TPD1, and from 7.7 ns to 8.1 ns on a TPD0. Because this technology operates at very low currents, capacitance presented by wire length is very critical at internal nodes. The ALS11 is part of a master bar design which does not lend itself to minimal line lengths. It is therefore believed that the gate-to-gate variation in delay is due directly to the differences in wire length, particularly those connecting the wired-AND input PNP transistors. (See Figure 1-7.)

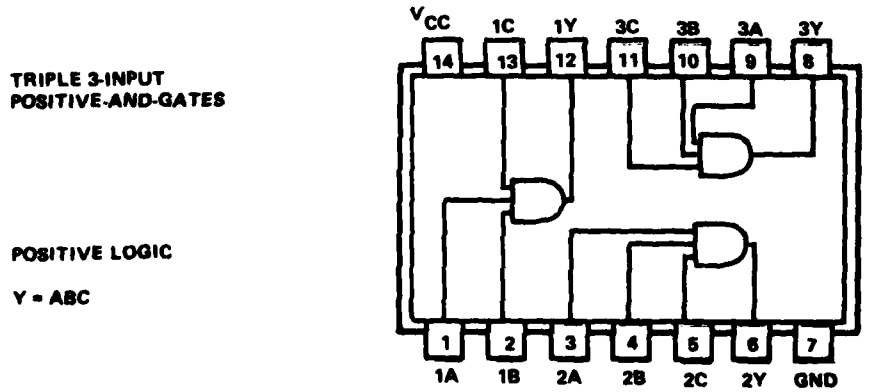


Figure 4-9. Functional Logic Diagram of the 54ALS11

Table 4-12. 5.0 V, 25°C, 50 pF
Average Performance/Power
54ALS11 vs 54LS11

Delay Path	54ALS11	54LS11
A - Y TPD1	11.7 ns	16.1 ns
A - Y TPD0	7.9 ns	14.0 ns
5.0 V DC Power/Pkg	6.3 mW	15.0 mW

As shown in Table 4-12, the 54ALS11 achieved a 27% speed improvement over the 54LS11 on a TPD1 delay. A 44% speed improvement was observed on a TPD0 delay. The 54ALS11 dissipated less than half the power of the 54LS11. At -55°C the 54ALS11 exhibited a minimum I_{OL} of 5.2 mA @ 0.5 volts, V_{OL} across ten (10) samples. (See page 62 Appendix B.) Two out of the ten part types tested had abnormally low I_{OS} currents of 38 and 46 mA, however, the average minimum I_{OS} @ +125°C T_j was 60 mA. (See I_{OUT} vs E_{OUT} (1) plot page 63 Appendix B.)

4.3.2 54ALS20

The 54ALS20 is a Dual 4-Input NAND gate in a 14 pin package. A logic diagram of this device is presented in Figure 4-10. Twenty-two (22) samples were tested at 25°C T_A and eight (8) samples at -55°C T_j and +125°C T_j.

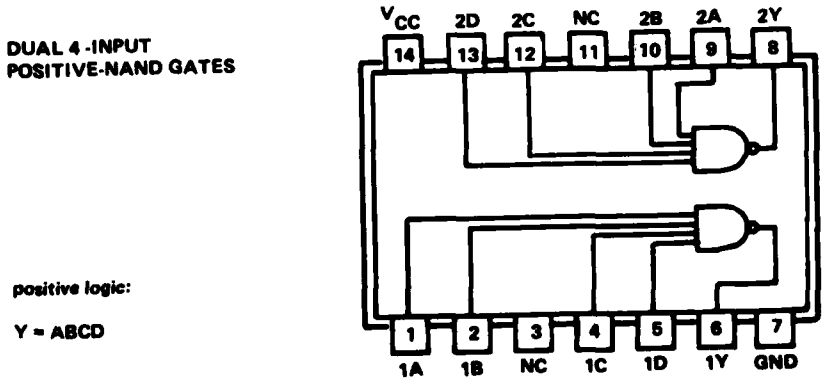


Figure 4-10. Functional Logic Diagram of the 54F20

The average room temperature ambient performance and power measured on this device is presented in Table 4-13. A comparison is also made to the equivalent 54LS20 at similar load conditions.

Table 4-13. 5.0 V, 25°C, 50 pF
Average Performance/Power
54ALS20 vs 54LS20

Delay Path	54ALS20	54LS20
A - Y TPDl	6.1 ns	6.8 ns
A - y TPDO	10.7 ns	15.7 ns
5.0 V DC Power/Pkg	3.4 mW	4.8 mW

Only a 10% speed improvement over the 54LS20 was observed on 54ALS20 TPDl delays, and a 32% speed improvement on TPDO delays. The 54ALS20 dissipated 29% less power than the 54LS20. At -55°C T_j the I_{OL} observed averaged 9.6 mA @ 0.5 V, V_{OL} (see page 68 Appendix B). The I_{OS} at +125°C T_j averaged 62 mA. (See page 69, Appendix B.)

4.3.3 54ALS74

The 54ALS74 is a Dual D-Type Flip-flop in a 14 pin package. A block diagram of the device is shown in Figure 4-11. Twenty-three (23) samples were examined at 25°C T_A and ten (10) samples at -55°C T_j and +125°C T_j. The average room temperature ambient performance and power observed are presented in Table 4-14. The 54ALS74 is also compared to the 54LS74 with similar load conditions.

Table 4-14. 5.0 V, 25°C, 50 pF
Average Performance/Power
54ALS74 vs 54LS74

Delay Path	54ALS74	54LS74
CLK-Q TPD1	8.9 ns	18.2 ns
CLK-Q TPD0	12.3 ns	27.0 ns
CLK-QBAR TPD1	9.3 ns	16.6 ns
CLK-QBAR TPD0	12.3 ns	26.7 ns
PSET-Q TPD1	7.8 ns	10.0 ns
PSET-QBAR TPD0	11.1 ns	19.6 ns
CLR-Q TPD0	10.5 ns	21.1 ns
CLR-QBAR TPD1	8.0 ns	9.8 ns
5.0 V DC Power/Pkg	9.0 mW	19 mW

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

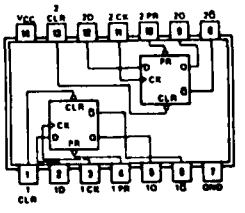


Figure 4-11. Functional Block Diagram of the 54ALS74

The 54ALS74 averages 42% faster delays than the 54LS74 over the eight paths shown in Table 4-14. Power dissipation was approximately 1/2 that of the 54LS74.

Room temperature miscellaneous performance parameters measured on the 54ALS74 are summarized in Table 4-15.

Table 4-15. 5.0 V, 25°C, 50 pF
54ALS74 Miscellaneous Performance Data

Parameter	Avg. Data
Set '0'	-3.5 ns
Set '1'	+4.0 ns
Hold '0'	-3.7 ns
Hold '1'	+3.4 ns
Minimum Positive CLK - PW	2.0 ns
Minimum Negative CLK - PW	8.4 ns
Minimum CLR - PW	1.9 ns
Minimum PR - PW	2.1 ns
CLR to CLK Recovery Time	1.0 ns
PR to CLK Recovery Time	.7 ns
Maximum Clock Frequency	52 MHz

The propagation delays over temperature and ±10% Vcc for the 54ALS74 can be found on pages 40, 41 and 42 of Appendix A. A 35% average performance degradation between 25°C T_A and +125°C T_j for a CLK-Q, QBAR TPD1 was measured. This abnormally high slowdown is an indication that the ALS74 is experiencing high temperature minority carrier storage. High temperature slowdown was also evident in the measurement of maximum clock frequency, F_{MAX}, which averaged 52 MHz at 25°C T_A but 31 MHz at +125°C T_j.

4.3.4 FEEDBACK DIODE PROBLEM

Figure 4-12 is a plot of the I_{out} vs E_{out} (o) characteristics of 3 different part types, the 54F20, the 54ALS20, and the 54ALS74. The characteristics of the 54F20 and the 54ALS20 indicate the presence of a feedback diode on each output (see Figures 1-7 and 1-8). The advantage of a feedback diode can be seen when a 30 ohm loadline (typical impedance of IBM's military multi-layer wiring boards) is drawn from a hypothetical 3.5 V output up level. The 54ALS74 which does not employ a feedback diode on its output shows the output sink current at ≈12 mA. The load line intersects the ALS74 output sink characteristic at 3.15 volts indicating that the largest incident falling voltage step from 3.5 volts is only 0.35 volts. Assuming that the 54ALS74 is driving an unterminated 30 ohm transmission line, and that the receiver is located at the end of the line, it would require seven (7) traversals up and down the line before the receiver input would fall below the 1.3 V ALS threshold.

The ALS20, on the other hand, which has an output feedback diode produces an incident voltage step of 1.25 volts (from 3.5 volts to 2.25 volts) and would take only one trip down the 30 ohms line to get the receiver input located at the end of the line to ≈1.0 volts, assuming that the high impedance of the receiver input causes doubling of the incident voltage step.

The 54F20 produces an incident voltage step of 1.5 volts (from 3.5 volts to 2.0 volts) and also would take only one trip down the 30 ohm line to drive the receiver input to ≈0.5 volts.

The photographs in Figures 4-13 and 4-14 will illustrate the actual occurrence of the 30 ohm transmission line effects hypothesized above. Figures 4-13(A) and 4-13(B) show the typical TPD0 and TPD1 of the 54ALS20 directly at the device or driver output pin. Figures 4-13(C) and 4-13(D) are pictures of the 54ALS20's TPDØ and TPD1 at the end of the 30 ohm unterminated transmission line. The step at the output of the driver results from two traversals up and down the line.

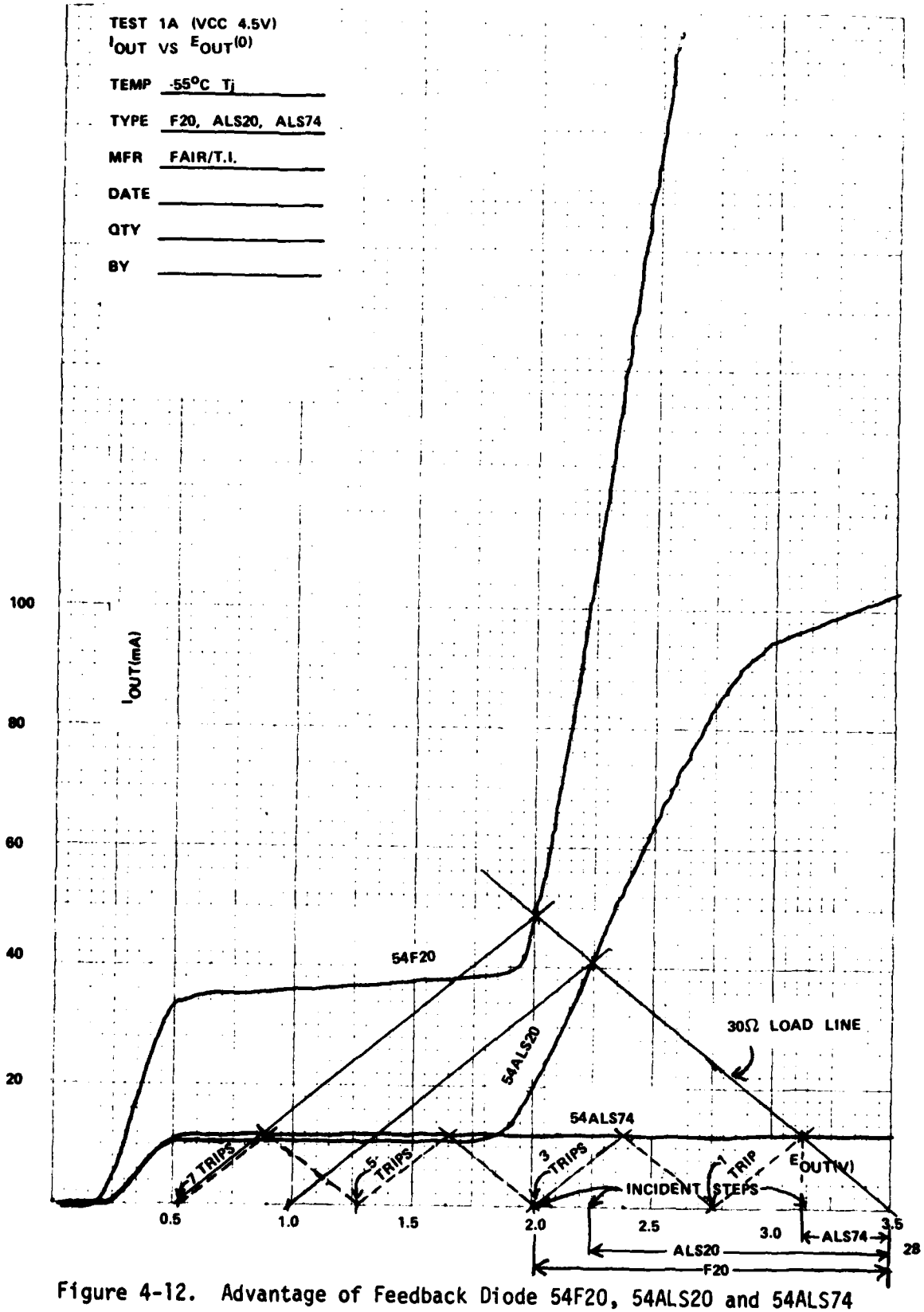
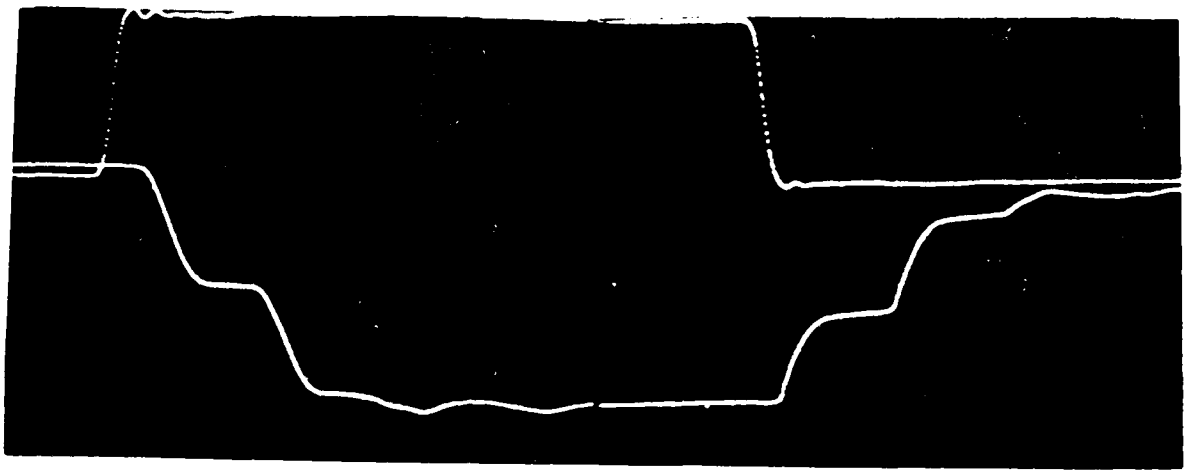
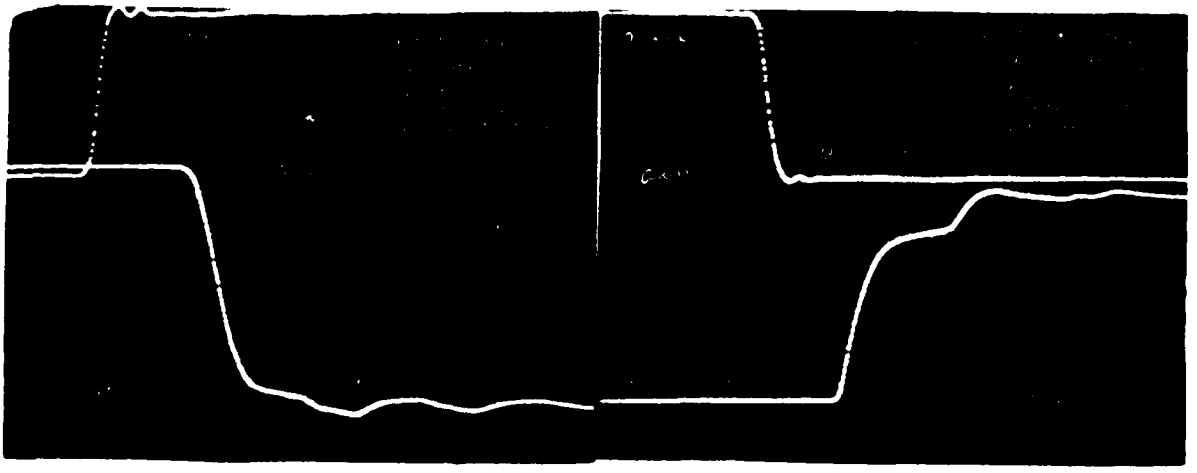


Figure 4-12. Advantage of Feedback Diode 54F20, 54ALS20 and 54ALS74

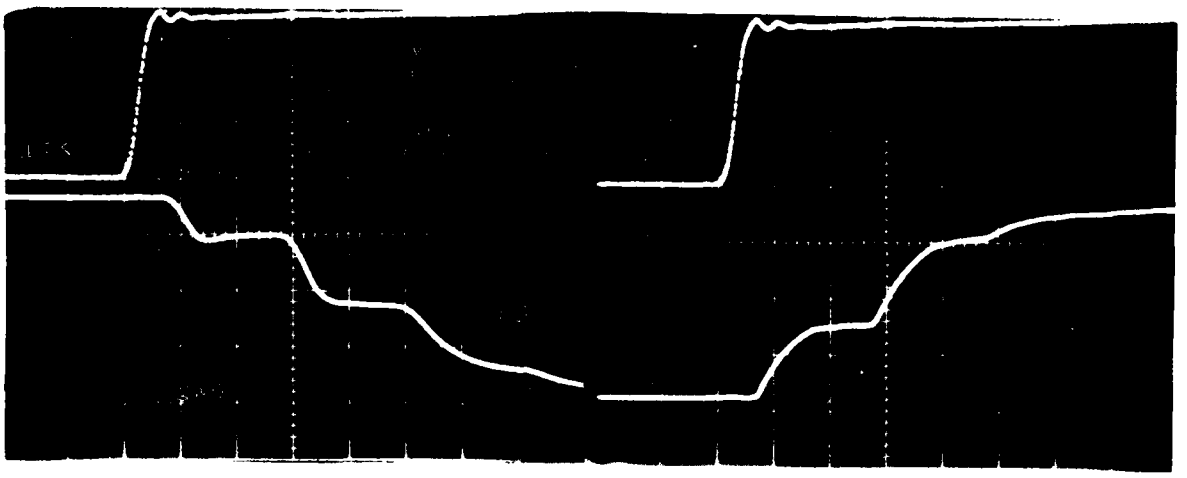


(A) TPD0 at the Output of the Driver (B) TPD1 at the Output of the Driver

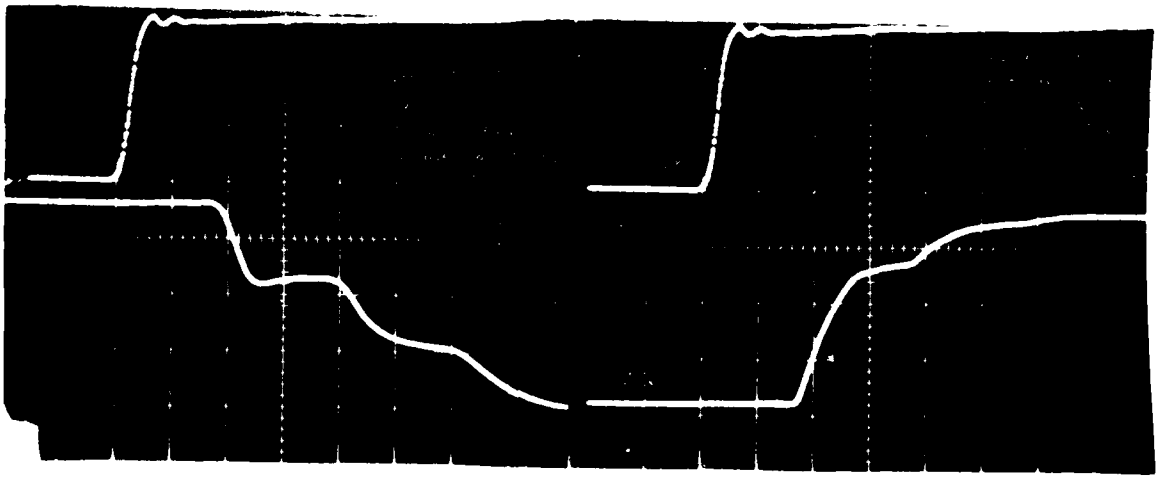


(C) TPD0 at the End of the Transmission Line (D) TPD1 at the End of the Transmission Line

Figure 4-13. ALS20 on a 30Ω Transmission Line



(A) TPD0 at the Output of the Driver (B) TPD1 at the Output of the Driver



(C) TPD0 at the End of the Transmission Line (D) TPD1 at the End of the Transmission Line

Figure 4-14. ALS74 on a 30 Transmission Line

Figures 4-14(A) and 4-14(B) are traces of the 54ALS74's TPDØ and TPD1 measured directly at the driver pin. Figures 4-14(C) and 4-14(D) are corresponding traces measured at the end of the 30 ohm line. The DC output sink characteristics of both the ALS20 and the ALS74 (see Figure 4-15) closely approximate and predict the AC characteristics pictured in Figures 4-13 and 4-14.

The 54ALS20 has an up level of 4.2 volts (See Figure 4-13). A 30 ohm load line drawn from this level to the intersection of the ALS20's I_{OL} characteristic predicts that an initial voltage step will occur at the output of the driver at B1 (See Figure 4-15) or 2.15 volts. This closely agrees with the first step on the TPD0 trace in Figure 4-13(A). This step which doubles by reflection at the end of the line is predicted to appear as a 4.1 volt step occurring at 0.1 volts or B2 (See Figure 4-15 and Figure 4-13(C)).

The 54ALS74 photographs in Figure 4-14 show an up level of approximately 3.6 volts. Three (3) voltage steps will occur at the output of the driver as indicated by points A1, A3, and A5 in Figure 4-15, and verified by Figure 4-14(A). Starting from an uplevel of 3.6 volts, the 30 ohms load line intersects the I_{OL} characteristic of the ALS74 at A1 or 2.98 volts. This agrees closely with the first step on the TPDØ trace in Figure 4-14(A). This incident step (.62 volts) doubles at the end of the line and appears as a 1.25 volt step occurring at 2.35 volts or A2. (See Figure 4-15 and Figure 4-14(C)). The incident voltage step (A1 Figure 4-15) at the output of the driver (.62 volts) waits for a reflected wave of 1.25 volts to travel from the end of the line to produce a 1.23 volt step at the driver output. This corresponds to the intersection of the 30 ohm load line and ALS74 I_{OL} characteristic at A3 or 1.75 volts. Figure 4-14(A) agrees closely with this prediction. A 0.6 volt wave (2.35V - 1.75V) travels back to the end of the line and doubles (1.2 volts) to produce a step at A4 or 1.15 volts. (See Figure 4-15 and Figure 4-14(C). The reflected wave of 1.2 volts from the end of the line travels back to the driver output to produce a step at A5 or 0.6 volts. The final traversal to the end of the line of a 0.55 volt wave doubles to produce a 1.1 volt step at A6 or 0.05 volts which is corroborated in Figure 4-14(C).

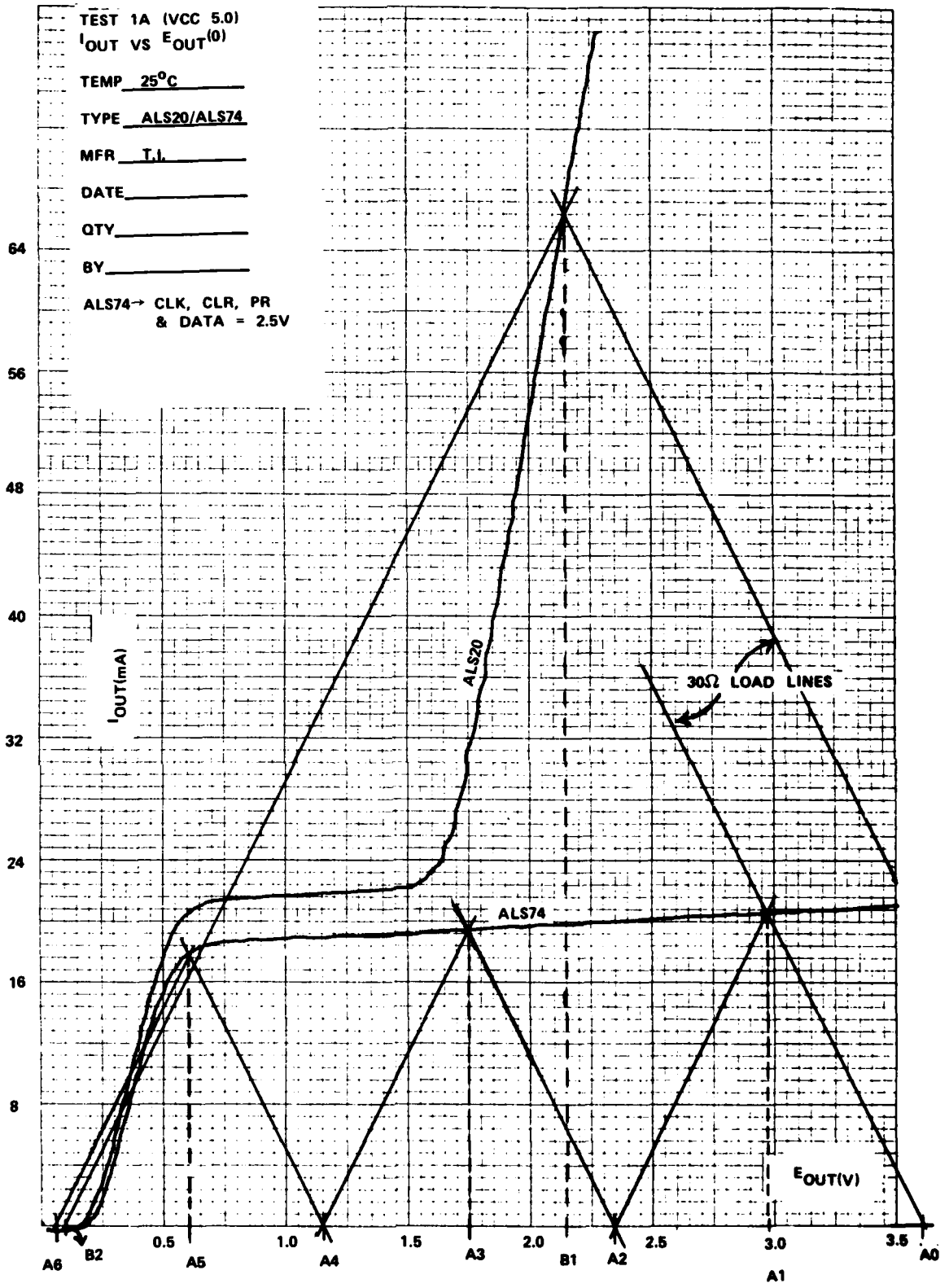


Figure 4-15. Feedback Diode vs No Feedback Diode I_{OUT} vs E_{OUT} (0) of ALS20 and ALS74

The above analysis shows that on 30 ohm transmission lines the TPDØ of the ALS74 without feedback diodes will require three (3) trips down, back, and down the line before a 1.3 V threshold is crossed for a receiver located at the end of the line. The ALS20 with feedback diodes requires one (1) trip. For receivers located at the output of the ALS74 driver four(4) traversals of the line are required to cross the 1.3 volt threshold. For the ALS20 two traversals are required to switch an ALS receiver located at the output of the driver.

A similar analysis can be made for LOW to HIGH (TPD1) transitions with the I_{OS} characteristics of the ALS20 and ALS74 shown in Figure 4-16. The I_{OS} characteristics of both parts are very similar. On a 30 ohm transmission line, the ALS74 presents a 1.4 volt step at the output of the driver and a 2.6 volt step at the end of the line corresponding to points A1 and A2 in Figure 4-16. This occurence is verified by the photographs in Figures 4-15(B) and 4-15(D). Likewise the ALS20 provides 47 mA source current to obtain a 1.65 volt incident step at B1, the output of the driver. This step doubles to produce a 3.4 volt step at the end of the transmission line, B2 (See Figure 4-16). The above occurrences are corroborated by Figures 4-13(B) and 4-13(D).

The preceding analysis shows that the I_{OS} characteristics of gate and flip-flop samples of the ALS family are marginally adequate on LOW to HIGH transitions to switch receivers located near the driver on the first incident step (assuming ALS threshold = 1.3 V). They will definitely provide an adequate step, (above threshold) due to the doubling of the reflected wave, for a receiver located at the end of a 30 ohm transmission line (for $V_{cc} \geq$ 5.0 volts).

The I_{OL} characteristics of the two ALS samples emphasize the importance of the output feedback diode in being able to guarantee that the receiver placed at the end of the line will switch on the initial step. On a TPDØ, ALS74 without the feedback diode to increase the output sink current requires 3 transitions up and down the 30 ohm line before the voltage level drops below the 1.3 V threshold. A receiver located near the ALS74 output would require 4 traversals of the transmission line to switch. The preceding analysis was

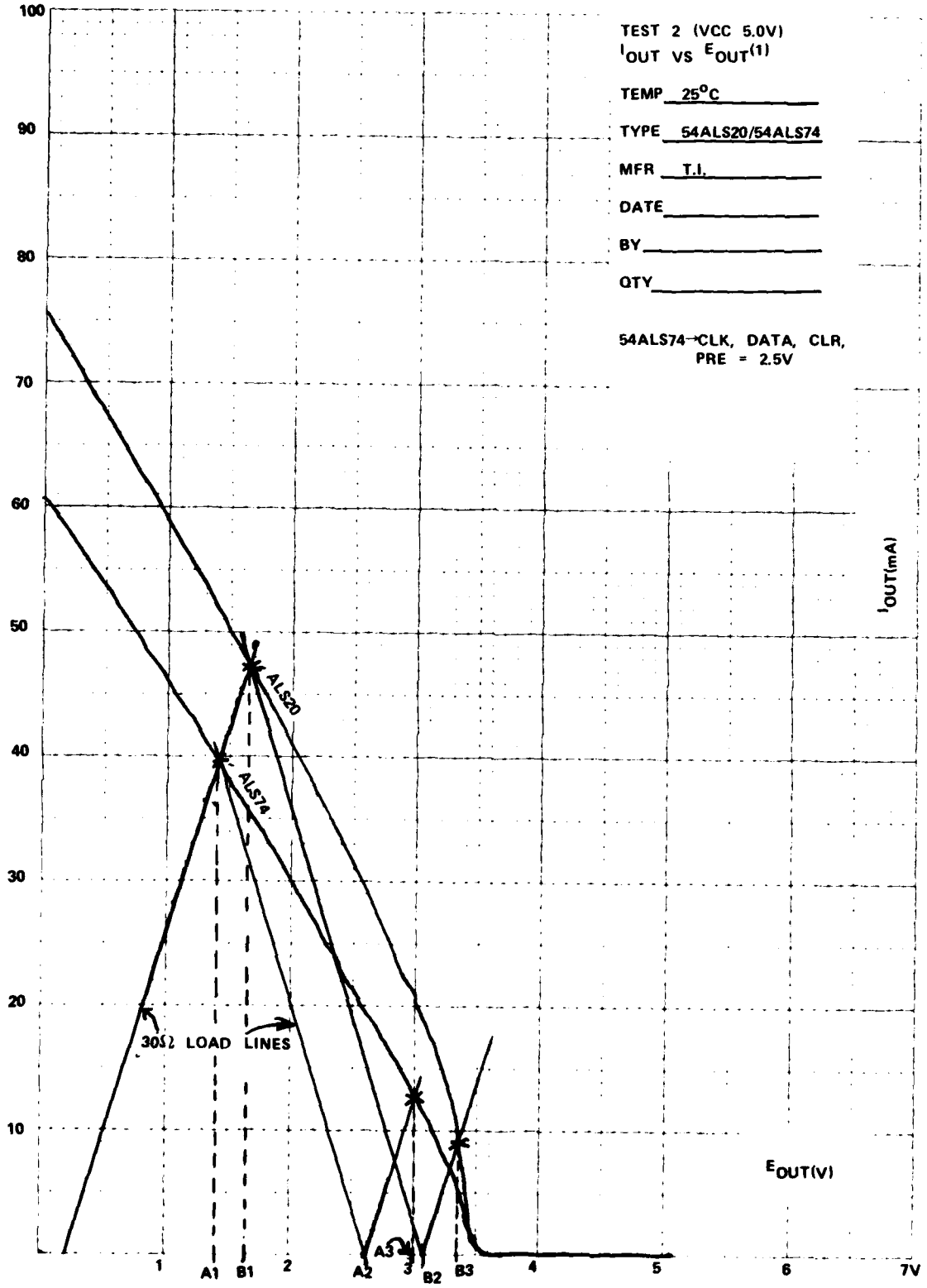


Figure 4-16. IOS Characteristic: ALS20 vs ALS74

done at room temperature, but at -55°C the problem is even more acute because the output sink current is even less (see Figures 4-12 and 4-15). TI has been consulted on the importance of a feedback diode in guaranteeing reflected wave switching in low impedance environments and has taken design steps to provide this on flip-flop outputs, and 3-state outputs. (Note the I_{OL} characteristic of the 54ALS574 on page 81, Appendix B does not have a feedback diode.) Three-state outputs, however, are provided with additional sink capability, specified at I_{OL} = 12 mA @ 0.5 V, -55°C Tj.

4.3.5 54ALS574

The 54ALS574 is an Octal D-Flip-flop with 3-state outputs in a 20 pin package. A logic diagram of this device appears in Figure 4-17. Thirty (30) samples were tested at 25°C T_A and ten (10) samples at -55°C T_j and +125°C T_j. Table 4-16 presents the 25°C average performance and power observed with the 54ALS574 versus similar performance of the 54LS374.

Table 4-16. 5.0 V, 25°C, 50 pF
Average Performance/Power
54ALS574 vs 54LS374

Delay Path	54ALS574	54LS374
CLK-Q TPD1	8.2 ns	18.9 ns
CLK-Q TPD0	10.5 ns	26.9 ns
TZL	11.6 ns	N/A*
TZH	11.1 ns	N/A*
TLZ	7.5 ns	N/A*
THZ	5.5 ns	N/A*
5.0 V DC Power/Pkg	66 mW	122 mW

* N/A - Not Available

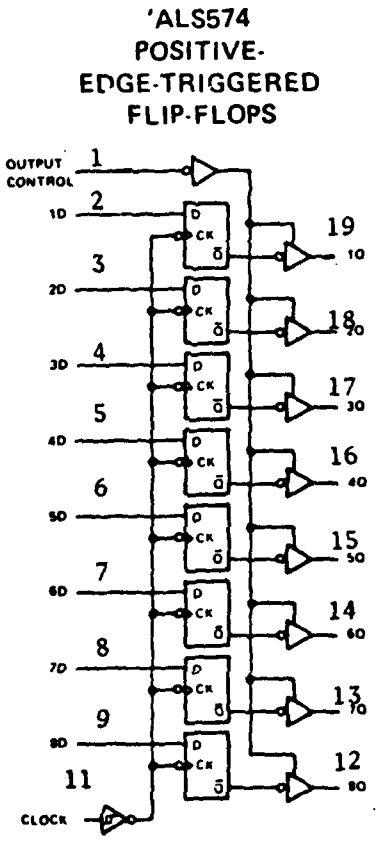


Figure 4-17. Functional Block Diagram of the 54ALS574

The 54ALS574 averages 58% faster delays than the 54LS374 at approximately 1/2 the power. AC parameters over the military temperature range are available on pages 43, 44, and 45 of Appendix A. The ALS574 did not operate at 4.5 V and 5.0 V, -55°C T_j; the outputs latched into 3-state mode. The data shown in Appendix A for -55°C was actually taken at a warmer temperature where the parts were able to work properly. In the DC analysis of the part, this anomaly was visible in the I_{out} vs. E_{out} (0) plot on page 81 of Appendix B. This characteristic which is normally plotted at 4.5 V, V_{cc} could not be plotted at -55°C T_j, unless V_{cc} was raised to $\geq$ 5.1 volts. As the output is swept from 0.0 to 3.5 volts, with V_{cc} less than 5.0 volts, the I_{OL} will drop from 30 mA @ 0.5 volts to 10 mA, from 0.6 volts to 3.5 volts on the output. Attempts to retrace the characteristic will put the output completely into a high impedance state in which no current either flows into or sources from the output. In discussing this phenomena with TI, it was learned that they were aware of the instability problem @ -55°C and had made appropriate design corrections. The source of the problem was an internal circuit not shown in the circuit schematic whose function was to cause the outputs of the 54ALS574 to become high impedance if the power supply voltage was grounded or lowered significantly. An improper resistor value was used in this circuit which caused the output to go into 3-state mode when $V_{cc} < 5.0$ volts. This low V_{cc} circuit safeguards bus applications, in which some devices connected to the bus might be powered-down but will not affect bus operation.

Section 5
CONCLUSIONS AND RECOMMENDATIONS

5.1 THE AS FAMILY

The test results from the 4 part types examined in the AS family by no means constitute a definitive or final description of the characteristics of this technology. This study was conducted during a period of development and definition for the AS product line. In most cases the samples examined in this study were first iteration product. IBM consulted with Texas Instrument during the course of this contract to inform the vendor of circuit anomalies detected in characterization. TI is in the process of modifying and adjusting circuit designs and fabrication processes to improve performance and correct design problems such as high temperature slowdown and input leakage observed on all part types.

In summary, however, the characterization results show the AS family to exhibit approximately 33% performance improvement over similar Schottky functions. The devices have the added advantage of higher complexity per package than existing Schottky. A slight power reduction under Schottky power was observed, averaging 14% across the four (4) parts tested. The AS family offers 3 types of output drive structures; Standard output, Buffer/ 3-State output, and Line Driver output. This study did not examine devices from the Line Driver category, because samples were unavailable. The input loading for all three (3) circuit types remain the same as Schottky. The input threshold of the AS family showed greater stability over the military temperature range than Schottky TTL, offering improved noise immunity. The input test conditions recommended in Section 3 of this report are the same as Schottky, except for threshold. IBM recommends that the DC characteristics outlined in Table 5-1 be used to specify the AS product line.

The I_{OL} characteristic of all AS part types should be able to guarantee reflected wave switching in low impedance (30 Ω) transmission line environments assuming feedback diodes are used on all outputs.

The I_{OS} characteristic of each category of AS parts is sufficient to guarantee incident wave switching on low impedance (30 Ω) transmission lines.

Table 5-1. Recommended DC Characteristics 54ASXX Family

Parameter	Standard	Buffer/3-State	Line Driver	Unit
Supply Voltage	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	V
I_{OH}	-2.0 max	-12.0 max	-40.0 max	mA
V_{OH}	2.5 min	2.4 min	2.0 min	V
I_{OL}	20.0 min	32.0 min	40.0 min	mA
V_{th}	1.3	1.3	1.3	V
I_{OS}	-120 min	-160 min	-200 min	mA
I_{IL}	-2.0 max	-2.0 max	-2.0 max	mA

I_{OH} = High Level Output current
V_{OH} = High Level Output Voltage @ I_{OH} max, V_{cc} = 4.5 volts
I_{OL} = Low Level Output current @ V_{OL} = 0.5 volts, V_{cc} = 4.5 volts
V_{th} = Input Threshold Voltage
I_{OS} = Output Short Circuit Current @ V_{OH} = 0.0 volts, V_{cc} = 5.5 volts
I_{IL} = Low Level Input Current @ V_{IL} = 0.5 volts, V_{cc} = 5.5 volts.

The announced AS product line consists of approximately 33 new, increased complexity, logic functions available in 20 to 28 pin dual inline and leadless chip carrier packages. Flatpacks are not presently being offered. Most functions are not pin-for-pin compatible with existing SSI and MSI Schottky functions, but instead offer similar functions at higher complexities, i.e., the 54AS804 is a Hex 2 Input NAND buffer vs the 54S37, a Quad 2-Input NAND buffer. Five (5) part types are presently available for commercial production orders. They are indicated in Table 5-2 which lists the planned AS product offerings. Some logically-equivalent Schottky functions are shown and a measure of the increased complexity provided by the AS function is indicated. As can be seen, the AS family is directed toward microprocessor interfacing, providing many byte-wide functions.

Table 5-2. AS Product Offering (Page 1 of 2)

	'AS TYPE		EQUIV. 54S/74S TYPE	EQUIV. FUNCT.
1.	'AS181	ARITHMETIC/LOGIC UNIT (ALU)*	'S181	1.0X
2.	'AS800	AND/NAND, TRIPLE 4-INPUT LINE DRIVER	'S00	1.8X
3.	'AS801	NAND, HEX 2-INPUT GATE	'S01	1.5X
4.	'AS802	OR/NOR, TRIPLE 4-INPUT LINE DRIVER	'S02	1.8X
5.	'AS804	NAND, HEX 2-INPUT LINE DRIVER*	'S04	1.5X
6.	'AS805	NOR, HEX 2-INPUT LINE DRIVER	NONE	-
7.	'AS808	AND, HEX 2-INPUT LINE DRIVER*	'S08	1.5X
8.	'AS820	NAND, DUAL 8-INPUT LINE DRIVER	'S20	2X
9.	'AS830	AND/NAND, 16-INPUT LINE DRIVER	'S30	2.5X
10.	'AS832	OR, HEX 2-INPUT LINE DRIVER	'S00	1.5X
11.	'AS836	EX-NOR, QUAD 2-INPUT LINE DRIVER	NONE	-
12.	'AS839	14-INPUT, 32-TERM, 6-OUTPUT FPLA	NONE	-
13.	'AS850	16-TO-1 MULTIPLEXER	'S150	1X
14.	'AS857	UNIVERSAL MULTIPLEXER	'S157/S158	3X
15.	'AS859	UNIVERSAL DECODER/DEMULTIPLEXER	'S138(259)	3X
16.	'AS867	8-BIT SYNCHRONOUS BI-DIRECTIONAL COUNTER	NONE	-
17.	'AS869	8-BIT SYNCHRONOUS BI-DIRECTIONAL COUNTER	'S169	2X
18.	'AS870	DUAL 16-WORD X 4-BIT REGISTER FILE	'S189A	2X
19.	'AS871	DUAL 16-WORD X 4-BIT REGISTER FILE	NONE	-
20.	'AS872	QUAD J-K FLIP-FLOP	'S112	2X
21.	'AS873	OCTAL TRANSPARENT LATCH	'S373	1.2X
22.	'AS874	OCTAL D-TYPE FLIP-FLOP	'S374	1.2X
23.	'AS875	QUAD D-TYPE FLIP-FLOP	'S74	2X
24.	'AS876	INVERTING 'AS874	NONE	-
25.	'AS877	OCTAL I/O STORING TRANSCEIVER	NONE	-
26.	'AS881	ARITHMETIC/LOGIC UNIT (ALU)*	'S181	1.05X
27.	'AS882	32-BIT FAST CARRY LOOK-AHEAD*	'S182	2.25X

*Available now for commercial production orders

Table 5-2. AS Product Offering (Page 2 of 2)

	'AS TYPE		EQUIV. 54S/74S TYPE	EQUIV. FUNCT.
28.	'AS883	19-BIT/18-BIT EXPANDABLE LATCHED PARITY	'S280	2X
29.	'AS884	DUAL 8-BIT EVEN PARITY	'S280	2X
30.	'AS885	8-BIT MAGNITUDE COMPARATOR	'S85	2.5X
31.	'AS886	EX-OR, HEX 2-INPUT LINE DRIVER	'S86	1.5X
32.	'AS888	8-BIT SLICE	'S481	2X
33.	'AS894	EXPANDABLE MULTIFUNCTION BINARY/ HEXADECIMAL SCALER	NONE	-

*Available now for commercial production orders.

5.2 THE ALS FAMILY

The ALS product line, like the AS family, is still in an early stage of development, although Texas Instruments has done more work with the ALS family than the AS. Three (3) of the four (4) part types examined in this study were first iteration products. The ALS74 was second iteration. TI presently is in the process of redesigning and relaying out many of its first designs to minimize wire lengths, optimize transistor geometries and incorporate feedback diodes on 3-state and flip-flop devices. Several master bar designs are being split into multiple bar designs. This study has helped to define many of these adjustments for the improvement of the product line.

Over the four (4) ALS part types tested an average 46% performance improvement over equivalent LS devices was observed. A similar percentage (47%) reduction in power was averaged over the four (4) part types tested. The ALS family offers three (3) types of output drive circuits. Standard, 3-State/Buffer and Line Driver. Three (3) standard part types and one 3-state device were tested. Input low current measured on all devices was less than 100 μA @ 0.2 volts. Output low current, I_{OL}, was similar to LS on the standard part types and higher on the 3-state device. All ALS devices averaged approxi-

mately 70 mA I_{OS}. IBM believes that this high I_{OS} characteristic is critical (see paragraph 4.4) to the performance of these low power circuits in low impedance transmission line environments. The ALS I_{OS} characteristic helps to guarantee reflected wave switching on LOW to HIGH transitions. The speed improvements achieved by these circuits has made it necessary that users consider transmission line effects when wiring ALS circuits on low impedance circuit boards. These effects discussed in Section 4 were highly unlikely with LS TTL because the slow rise and fall times of LS TTL did not, in most applications, approximate the time it took the LS signal to travel through the wiring medium. In low-impedance environments feedback diodes are extremely important to the propagation delay of ALS circuits to the logical '0' state as demonstrated in paragraph 4.3.4. They will help to guarantee reflected wave switching. IBM recommends that TI use feedback diodes on outputs of all ALS parts (except open collector). It is recommended that the DC characteristics shown in Table 5-3 be used to define the ALS product line.

Table 5-3. Recommended DC Characteristcs
54ALSXX Family

Parameter	Standard	3/State/Buffer	Line Driver	Units
Supply Voltage	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	V
I_{OH}	-0.4 max	-1.0 max	-12.0 max	MA
V_{OH}	2.5 min	2.4 min	2.0 min	V
I_{OL}	6 min	12 min	12 min	MA
Vth	1.3	1.3	1.3	V
I_{OS}	-60 min	-70 min	-120 min	MA
I_{IL}	-0.2 max	-0.2 max	-0.2 max	MA

I_{OH} = High Level Output current
V_{OH} = High Level Output Voltage @ I_{OH} max, Vcc = 4.5 volts
I_{OL} = Low Level Output current @ V_{OL} = 0.5 volts, Vcc = 4.5 volts.
V_{th} = Input Threshold Voltage.
I_{OS} = Output Short Circuit Current @ V_{OH} = 0.0 volts, Vcc = 5.5 volts.
I_{IL} = Low Level Input Current @ V_{IL} = 0.5 volts, Vcc = 5.5 volts.

Table 5-4 lists the ALS product line presently planned by TI. Approximately 107 unique functions are planned, and functions range from simple gates to registered gate arrays. Most functions are pin-for-pin replacable LS functions, however, many are new higher complexity functions. Included in this list are seven distinct part types labeled ALS1000-ALS1032. TI has designed these gate functions with higher I_{OL} characteristics than the standard ALS equivalent. Their output DC characteristics are expected to be similar to FAST. Power dissipation of this ALS1000 series is purported to be less than the FAST equivalent with slightly slower performance. Samples of ALS1000 series circuits will be available in 1Q81. ALS products are available in 14 to 28 pin dual inline and 20 to 28 pin leadless chip carrier packages. Flatpacks are not presently being offered. Twenty-eight (28) part types are presently available for commercial production orders. They are indicated in Table 5-4.

5.3 THE FAST FAMILY

The FAST product line is a more mature product line than either AS or ALS. Part types examined under this contract were generally second and/or third iteration designs. Fairchild has gone through the process of splitting up master bar designs, optimizing transistor and diode geometries, correcting design problems, and incorporating performance enhancement ideas on many part types.

Over the five (5) part types tested, there was an average performance improvement over equivalent Schottky devices of 43%. The average percentage power reduction under Schottky was 71%.

Table 5-4. ALS Product Offering (Page 1 of 3)

	DEVICE	DESCRIPTION
1.	54/74ALS00	QUAD 2-INPUT NAND GATES*
2.	54/74ALS01	QUAD 2-INPUT NAND GATES, O.C.*
3.	54/74ALS02	QUAD 2-INPUT NOR GATES*
4.	54/74ALS03	QUAD 2-INPUT NAND GATES*
5.	54/74ALS04	HEX INVERTER*
6.	54/74ALS05	HEX INVERTER, O.C.*
7.	54/74ALS08	QUAD 2-INPUT AND GATES*
8.	54/74ALS09	QUAD 2-INPUT AND GATES, O.C.*
9.	54/74ALS10	TRIPLE 3-INPUT NAND GATES, O.C.*
10.	54/74ALS11	TRIPLE 3-INPUT AND GATES*
11.	54/74ALS12	TRIPLE 3-INPUT NAND GATES, O.C.*
12.	54/74ALS15	TRIPLE 3-INPUT AND GATES, O.C.*
13.	54/74ALS20	DUAL 4-INPUT NAND GATES*
14.	54/74ALS21	DUAL 4-INPUT AND GATES*
15.	54/74ALS22	DUAL 4-INPUT NAND GATES, O.C.*
16.	54/74ALS27	TRIPLE 3-INPUT NOR GATES*
17.	54/74ALS28	QUAD 2-INPUT NOR BUFFERS*
18.	54/74ALS30	8-INPUT POSITIVE NAND GATES*
19.	54/74ALS32	QUAD 2-INPUT NOR GATES*
20.	54/74ALS33	QUAD 2-INPUT NOR BUFFERS, O.C.*
21.	54/74ALS37	QUAD 2-INPUT NAND BUFFERS*
22.	54/74ALS38	QUAD 2-INPUT NAND BUFFERS, O.C.*
23.	54/74ALS40	DUAL 4-INPUT NAND BUFFERS*
24.	54/74ALS74	DUAL D-TYPE FLIP-FLOPS*
25.	54/74ALS86	QUAD 2-INPUT EXCLUSIVE OR GATES
26.	54/74ALS109	DUAL JK FLIP-FLOPS*
27.	54/74ALS112	DUAL JK FLIP-FLOPS*
28.	54/74ALS113	DUAL JK FLIP-FLOPS*
29.	54/74ALS114	DUAL JK FLIP-FLOPS*
30.	54/74ALS133	13-INPUT NAND GATE*
31.	54/74ALS138	3-TO-8 LINE DECODER/DEMULTIPLEXER
32.	54/74ALS139	DUAL 2-TO-4 LINE DECODERS/DEMULTIPLEXERS
33.	54/74ALS151	1-OF-8 DATA SELECTORS/MULTIPLEXERS
34.	54/74ALS153	DUAL 4-LINE-TO-1-LINE DATA SELECTORS/ MULTIPLEXERS
35.	54/74ALS157	QUAD 2-TO-1-LINE DATA SELECTOR/MULTIPLEXERS
36.	54/74ALS158	QUAD 2-TO-1-LINE DATA SELECTOR/ MULTIPLEXERS
37.	54/74ALS160	DECADE SYNCHRONOUS 4-BIT COUNTER, DIRECT CLEAR
38.	54/74ALS161	BINARY SYNCHRONOUS 4-BIT COUNTER, DIRECT CLEAR
39.	54/74ALS162	DECADE SYNCHRONOUS 4-BIT COUNTER, SYNC. CLEAR
40.	54/74ALS163	BINARY SYNCHRONOUS 4-BIT COUNTER, SYNC. CLEAR

* Available now for commercial production orders.

Table 5-4. ALS Product Offering (Page 2 of 3)

	DEVICE	DESCRIPTION
41.	54/74ALS168	4-BIT UP/DOWN DECADE COUNTER
42.	54/74ALS169	4-BIT UP/DOWN BINARY COUNTER
43.	54/74ALS175	QUAD D-TYPE FLIP-FLOPS
44.	54/74ALS190	SYNC. UP/DOWN BCD COUNTER
45.	54/74ALS191	SYNC. UP/DOWN BINARY COUNTER
46.	54/74ALS192	SYNC. UP/DOWN BCD COUNTER
47.	54/74ALS193	SYNC. UP/DOWN BINARY COUNTER
48.	54/74ALS240	OCTAL INV. BUS/LINE DRIVERS
49.	54/74ALS241	OCTAL BUS/LINE DRIVERS
50.	54/74ALS242	QUAD BUS TRANSCEIVERS
51.	54/74ALS243	QUAD BUS TRANSCEIVERS
52.	54/74ALS244	OCTAL BUS/LINE DRIVER
53.	54/74ALS251	8-INPUT MULTIPLEXER, 3-STATE
54.	54/74ALS253	DUAL DATA SELECTORS/MULTIPLEXERS, 3-STATE
55.	54/74ALS257	QUAD 2-INPUT MULTIPLEXER, 3-STATE
56.	54/74ALS258	QUAD 2-INPUT MULTIPLEXER, 3-STATE
57.	54/74ALS299	OCTAL SHIFT/STORAGE REGISTER, 3-STATE
58.	54/74ALS323	OCTAL SHIFT/STORAGE REGISTER, 3-STATE
59.	54/74ALS352	DUAL 4-LINE TO 1-LINE DATA SELECTORS/ MULTIPLEXERS
60.	54/74ALS353	DUAL 4-LINE TO 1-LINE DATA SELECTORS/ MULTIPLEXERS
61.	54/74ALS465	OCTAL BUFFERS, 3-STATE
62.	54/74ALS466	INV. OCTAL BUFFERS, 3-STATE
63.	54/74ALS467	OCTAL BUFFER, 3-STATE
64.	54/74ALS468	INV. OCTAL BUFFER, 3-STATE
65.	54/74ALS521	OCTAL COMPARATOR
66.	54/74ALS538	1-OF-8 DECODER, 3-STATE
67.	54/74ALS539	DUAL 1-OF-4 DECODER, 3-STATE
68.	54/74ALS540	OCTAL INV. BUS/LINE DRIVERS
69.	54/74ALS541	OCTAL BUS/LINE DRIVERS
70.	54/74ALS560	4-BIT DECADE COUNTER, 3-STATE
71.	54/74ALS561	4-BIT BINARY COUNTER, 3-STATE
72.	54/74ALS568	4-BIT DECADE COUNTER, 3-STATE
73.	54/74ALS569	4-BIT BINARY COUNTER, 3-STATE
74.	54/74ALS573	OCTAL D TYPE LATCHES*
75.	54/74ALS574	OCTAL D TYPE FLIP-FLOPS*
76.	54/74ALS576	INV. OCTAL D TYPE FLIP-FLOPS*
77.	54/74ALS580	INV. OCTAL D-TYPE LATCHES*
78.	54/74ALS620	INV. OCTAL BUS TRANSCEIVER, DUAL 3-STATE
79.	54/74ALS621	OCTAL BUS TRANSCEIVERS, DUAL ENABLE
80.	54/74ALS622	INV. OCTAL BUS TRANSCEIVERS, DUAL ENABLE

* Available now for commercial production orders.

Table 5-4. ALS Product Offering (Page 3 of 3)

	DEVICE	DESCRIPTION
81.	54/74ALS623	OCTAL BUS TRANSCEIVERS, DUAL 3-STATE
82.	54/74ALS638	INV. OCTAL BUS TRANSCEIVERS, 3-STATE AND O.C.
83.	54/74ALS639	INV. OCTAL BUS TRANSCEIVERS, 3-STATE AND O.C.
84.	54/74ALS640	INV. OCTAL BUS TRANSCEIVERS, 3-STATE
85.	54/74ALS641	OCTAL BUS TRANSCEIVER, O.C.
86.	54/74ALS642	INV. OCTAL BUS TRANSCEIVER, O.C.
87.	54/74ALS643	INV./TRUE OCTAL BUS TRANSCEIVER, 3-STATE
88.	54/74ALS644	INV./TRUE OCTAL BUS TRANSCEIVER, O.C.
89.	54/74ALS645	OCTAL BUS TRANSCEIVER
90.	54/74ALS857	UNIVERSAL MULTIPLEXER
91.	54/74ALS873	OCTAL TRANSPARENT LATCH*
92.	54/74ALS874	OCTAL D-TYPE FLIP-FLOP*
93.	54/74ALS876	INV. OCTAL D-TYPE FLIP-FLOP*
94.	54/74ALS880	INV. OCTAL TRANSPARENT LATCH*
95.	54/74ALS1000	BUFFER 00 GATE ('ALS37)
96.	54/74ALS1002	BUFFER 02 GATE ('ALS28)*
97.	54/74ALS1003	BUFFER 03 GATE*
98.	54/74ALS1008	BUFFER 08 GATE*
99.	54/74ALS1010	BUFFER 10 GATE*
100.	54/74ALS1011	BUFFER 11 GATE*
101.	54/74ALS1020	BUFFER 20 GATE ('ALS40)*
102.	54/74ALS1032	BUFFER 32 GATE*
103.	54/74ALS1616	16 x 16 MULTIPLIER
104.	54/74ALS16L8	OCTAL 16-INPUT AND-OR-INVERT GATE ARRAY
105.	54/74ALS16R8	OCTAL 16-INPUT REGISTERED AND-OR GATE ARRAY
106.	54/74ALS16R6	HEX 16-INPUT REGISTERED AND-OR GATE ARRAY
107.	54/74ALS16R4	QUAD 16-INPUT REGISTERED AND-OR GATE ARRAY

* Available now for commerical production orders.

The FAST family offers improved input loading characteristics, with the average I_{IL} of the five part types tested measuring less than 0.6 mA @ 0.2 volts. The I_{OL} characteristic of the FAST family is similar to that of Schottky TTL with an added advantage of feedback diodes to increase the current sinking capability of the output transistor. As a result FAST devices guarantee reflected wave switching during High to Low transitions (TPDØ) on low impedance (30 Ω) wiring boards (as shown in paragraph 4.3.4). The I_{OS} characteristic of FAST devices is very similar to that of Standard ALS part types, averaging 85 mA. Reflected wave switching on TPD1's in low impedance (30 Ω) environments is also guaranteed by this characteristic.

It is recommend that the DC characteristics in Table 5-5 be used to define the FAST family.

Fairchild has announced a family of 88 part types, most of which are pin-for-pin compatible with Schottky functions. New logic functions are included along with multiplier functions, a scratch pad memory, and memory peripheral functions. The product line and description are listed in Table 5-6. Thirty-seven (37) part types are presently available for production orders at both military and commercial specifications. FAST parts are available in dual-in-line, flatpack, and leadless chip carrier packages.

Table 5-5. Recommended DC Characteristics
FAST (54FXX) Family

PARAMETER	SPECIFICATION	UNITS Supply
Voltage	4.5 to 5.5	V
I_{OH}	-1.0 max	mA
V_{OH}	2.55 min	V
I_{OL}	20.0 min	mA
V_{th}	1.5	V
I_{OS}	-60.0 min	mA
I_{IL}	0.6 max	mA

TEST CONDITIONS:

I_{OH} = High Level Output current

V_{OH} = High Level Output Voltage @ I_{OH} max, V_{cc} = 4.5 volts

I_{OL} = Low Level Output current @ V_{OL} = 0.5 volts, V_{cc} = 4.5 volts

V_{th} = Input Threshold Voltage

I_{OS} = Output Short Circuit Current @ V_{OH} = 0.0 volts, V_{cc} = 5.5 volts

I_{IL} = Low Level Input Current @ V_{IL} = 0.5 volts, V_{cc} = 5.5 volts

Table 5-6. FAST Product Offering (Page 1 of 2)

	DEVICE	DESCRIPTION
1.	54F/74F00	Quad 2-Input NAND Gate *
2.	54F/74F02	Quad 2-Input NOR Gate *
3.	54F/74F04	Hex Inverter *
4.	54F/74F08	Quad 2-Input AND Gate *
5.	54F/74F10	Triple 3-Input NAND Gate *
6.	54F/74F11	Triple 3-Input AND Gate *
7.	54F/74F20	Dual 4-Input NAND Gate *
8.	54F/74F32	Quad 2-Input OR Gate *
9.	54F/74F64	AND/OR - Invert Gate *
10.	54F/74F74	Dual D-Type Flip-Flop
11.	54F/74F86	Quad 2-Input Exlusive-OR Gate *
12.	54F/74F109	Dual JK Flip-Flop *
13.	54F/74F112	Dual JK Flip-Flop
14.	54F/74F113	Dual JK Flip-Flop
15.	54F/74F114	Dual JK Flip-Flop
16.	54F/74F138	One-of-Eight Decoder/Demultiplexer *
17.	54F/74F139	Dual One-of-Four Decoder/Demultiplexer *
18.	54F/74F151	8-Input Multiplexer *
19.	54F/74F153	Dual 4-Input Multiplexer *
20.	54F/74F157	Quad 2-Input Multiplexer *
21.	54F/74F158	Quad 2-Input Multiplexer *
22.	54F/74F160	BCD Decade Ctr. Asyn. Reset
23.	54F/74F161	4-Bit Binary Ctr. Asyn. Reset
24.	54F/74F162	BCD Decade Ctr. Synch. Reset
25.	54F/74F163	4-Bit Binary Ctr. Synch. Reset
26.	54F/74F168	Up/Down Decade Counter
27.	54F/74F169	Up/Down Binary Counter
28.	54F/74F175	Quad D Flip-Flop w/Common Master Reset*
29.	54F/74F181	Arithmetic Logic Unit *
30.	54F/74F182	Carry Look-Ahead Generator
31.	54F/74F189	64-Bit Memory 3-State
32.	54F/74F190	Up/Down Decade Counter *
33.	54F/74F191	Up/Down Binary Counter *
34.	54F/74F192	Up/Down Decade Counter
35.	54F/74F193	Up/Down Binary Counter
36.	54F/74F194	4-Bit Bidirectional Universal Shift Register *
37.	54F/74F240	Octal Inv. Bus/Line Driver
38.	54F/74F241	Octal Bus/Line Drive *
39.	54F/74F242	Quad Bus Transceiver
40.	54F/74F243	Quad Bus Transceiver
41.	54F/74F244	Octal Bus/Line Driver *
42.	54F/74F245	Octal Bus Transceiver
43.	54F/74F251	8-Input Multiplexer 3-State *
44.	54F/74F253	Dual 4-Input Multiplexer 3-State *
45.	54F/74F257	Quad 2-Input Multiplexer 3-State *

*Available now for military and commercial production orders.

Table 5-6. FAST Product Offering (Page 2 of 2)

	DEVICE	DESCRIPTION
46.	54F/74F258	Quad 2-Input Multiplexer 3-State *
47.	54F/74F280	9-Bit Parity Generator/Checker
48.	54F/74F283	4-Bit Full Adder
49.	54F/74F289	64-Bit Memory Open Collector
50.	54F/74F299	Octal Shift/Storage Register 3-State
51.	54F/74F322	Octal Shift/Storage Register 3-State
52.	54F/74F323	Octal Shift/Storage Register 3-State
53.	54F/74F350	4-Bit Shifter; 3-State Outputs *
54.	54F/74F352	Dual 4-Input Multiplexer (Invered '153)
55.	54F/74F353	Dual 4-Input Multiplexer 3-State (Inverted '253) *
56.	54F/74F373	Octal D Latch *
57.	54F/74F374	Octal D Flip-Flop *
58.	54F/74F379	Quad D Flip-Flop with Enable
59.	54F/74F381	Arithmetic Logic Unit
60.	54F/74F382	Arithmetic Logic Unit
61.	54F/74F385	Quad Serial Adder/Subtractor
62.	54F/74F398	4-Bit Flip-Flop
63.	54F/74F399	4-Bit Flip-Flop
64.	54F/74F500	A/D Flash Convertor
65.	54F/74F521	Octal Comparator *
66.	54F/74F524	Register Comparator
67.	54F/74F533	Inverting Octal D Latch *
68.	54F/74F534	Inverting Octal Flip-Flop
69.	54F/74F537	One-of-Ten Decoder; 3-State Outputs
70.	54F/74F538	One-of-Eight Decoder; 3-State Outputs
71.	54F/74F539	Dual One-of-Four Decoder; 3-State Outputs
72.	54F/74F545	Octal Bus Transceiver
73.	54F/74F550	Registered Transceiver (AMD2950)
74.	54F/74F551	Registered Transceiver (AMD2951)
75.	54F/74F552	Octal Registered Transceiver with parity and flag
76.	54F/74F553	Octal Registed Transceiver w/parity
77.	54F/74F557	8 x 8 Multiplier with Latch
78.	54F/74F558	8 x 8 Multiplier
79.	54F/74F559	8-Bit Multiplier/Divider
80.	54F/74F568	4-Bit Binary Counter; 3-State Outputs
81.	54F/74F569	4-Bit Decade Counter; 3-State Outputs
82.	54F/74F588	GPIB Compatible Octal Transceiver
83.	54F/74F610	Memory Mapper; Latched, 3-State Outputs
84.	54F/74F611	Memory Mapper; Latched, O/C Outputs
85.	54F/74F612	Memory Mapper; 3-State Outputs
86.	54F/74F613	Memory Mapper; O/C Outputs
87.	54F/74F630	Memory Error Detector/Corrector; 3-State
88.	54F/74F631	Memory Error Detector/Corrector O/C

*Available now for military and commercial production orders.

5.4 SECOND SOURCE ACTIVITY

National has announced that they will second source the AS and ALS product lines. Samples are to be available in 4Q81. Motorola has announced that they will second source the ALS product line, with samples available in 2Q81. The FAST product line will be second sourced by Signetics and Motorola samples to be available in 4Q81.

5.5 TEST RECOMMENDATIONS

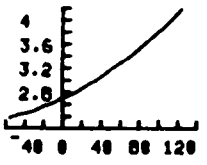
IBM recommends that the input test conditions, AC measurement points, circuit thresholds, and test load configurations outlined in Section 3 of this report be used on future MIL-M-38510 Detailed Specifications of circuits from each of the logic families studied.

APPENDIX A

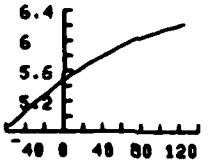
AC CHARACTERIZATION DATA

CIRCUIT TYPE TEXAS INSTR. AS804 10/08/88 11:21:18

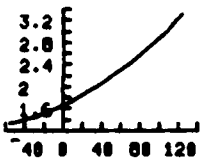
DELAY PATH	LOAD	50	PF	5.0	VOLTS					
	MINIMUM			AVERAGE			MAXIMUM			
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C	
1A-1Y 50PF TPD1	2.3	2.8	4.0	2.4	2.9	4.2	2.4	3.1	4.4	
1A-1Y 50PF TPD0	3.0	3.1	3.4	3.0	3.2	3.4	3.1	3.2	3.5	
2A-2Y 150PF TPD1	3.3	3.7	5.5	3.3	3.9	5.9	3.4	4.2	6.2	
2A-2Y 150PF TPD0	4.8	5.1	5.4	4.9	5.7	6.2	4.9	6.6	7.1	
3A-3Y 250PF TPD1	4.1	4.6	6.7	4.2	4.8	7.0	4.3	5.2	7.4	
3A-3Y 250PF TPD0	6.1	6.2	6.6	6.2	6.3	6.8	6.8	6.7	7.0	
4A-4Y 30X TPD1	1.2	1.7	3.0	1.3	1.9	3.3	1.7	2.3	3.6	
4A-4Y 30X TPD0	1.9	2.0	2.1	2.2	2.2	2.3	2.3	2.4	2.4	
T-RISE 50PF	1.2	1.2	1.5	1.2	1.3	1.6	1.2	1.4	1.7	
T-FALL 50PF	1.0	2.0	2.4	1.9	2.1	2.4	1.9	2.2	2.5	
Δ 30X-50PF TPD1	.7	.6	.5	1.1	1.0	.9	1.2	1.1	1.0	
Δ 30X-50PF TPD0	.7	.8	1.0	.8	.9	1.1	1.1	1.2	1.3	



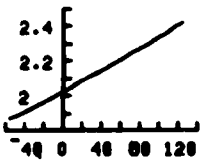
1A-1Y 50PF TPD1



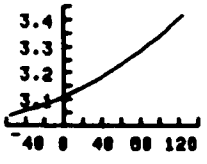
2A-2Y 150PF TPD0



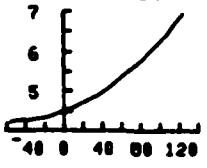
4A-4Y 30X TPD1



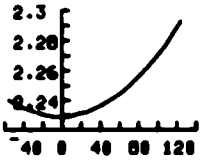
T-FALL 50PF



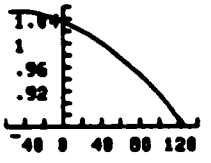
1A-1Y 50PF TPD0



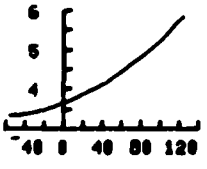
3A-3Y 250PF TPD1



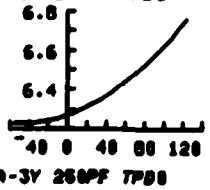
4A-4Y 30X TPD0



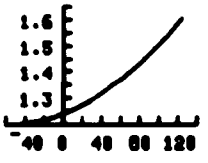
Δ 30X-50PF TPD1



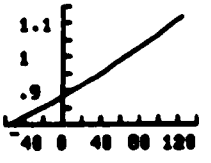
2A-2Y 150PF TPD1



3A-3Y 250PF TPD0



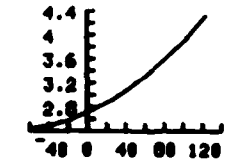
T-RISE 50PF



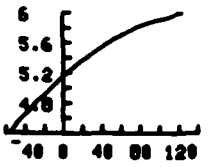
Δ 30X-50PF TPD0

CIRCUIT TYPE TEXAS INSTR. AS864 10/08/80 11:19:32

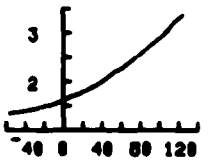
DELAY PATH	LOAD 50 PF 4.5 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
1A-1Y 50PF TPD1	2.4	2.8	4.1	2.4	2.9	4.3	2.5	3.1	4.6
1A-1Y 50PF TPD0	2.8	2.9	3.1	2.8	2.9	3.2	2.9	3.8	3.3
2A-2Y 150PF TPD1	3.6	3.9	5.0	3.7	4.1	6.1	3.7	4.3	6.5
2A-2Y 150PF TPD0	4.3	4.7	5.2	4.4	5.4	6.0	4.5	6.6	6.9
3A-3Y 250PF TPD1	4.5	5.0	6.9	4.6	5.1	7.3	4.7	5.5	7.9
3A-3Y 250PF TPD0	5.6	5.8	6.3	5.7	6.0	6.5	6.6	6.4	6.7
4A-4Y 30X TPD1	1.2	1.7	3.1	1.3	1.8	3.4	1.7	2.2	3.7
4A-4Y 30X TPD0	1.9	1.9	1.9	2.2	2.2	2.2	2.2	2.3	2.3
T-RISE 50PF	1.2	1.3	1.7	1.3	1.3	1.7	1.3	1.4	1.8
T-FALL 50PF	1.6	1.8	2.2	1.6	1.9	2.3	1.6	1.9	2.3
Δ 30X-50PF TPD1	.8	.8	.6	1.1	1.1	.9	1.2	1.2	1.1
Δ 30X-50PF TPD0	.6	.7	.9	.7	.8	1.0	.9	1.0	1.3



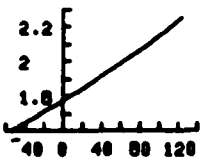
1A-1Y 50PF TPD1



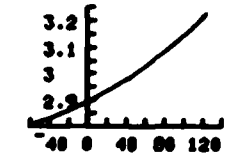
2A-2Y 150PF TPD0



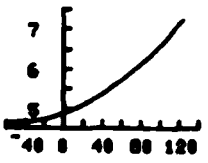
4A-4Y 30X TPD1



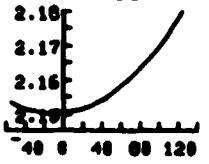
T-FALL 50PF



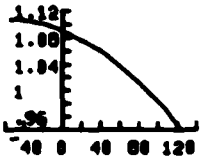
1A-1Y 50PF TPD0



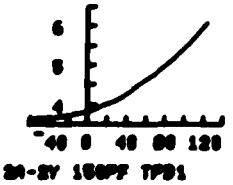
3A-3Y 250PF TPD1



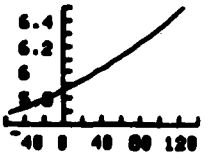
4A-4Y 30X TPD0



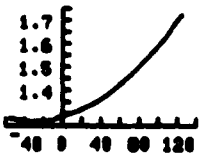
Δ 30X-50PF TPD1



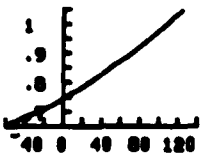
2A-2Y 150PF TPD1



3A-3Y 250PF TPD0



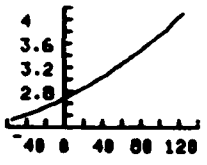
T-RISE 50PF



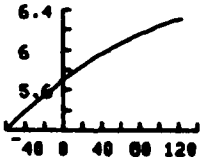
Δ 30X-50PF TPD0

CIRCUIT TYPE TEXAS INSTR. AS804 10/08/80 11:22:48

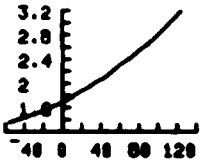
DELAY PATH	LOAD 50 PF 5.5 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
1A-1Y 50PF TPD1	2.3	2.8	3.9	2.3	2.9	4.1	2.4	3.1	4.4
1A-1Y 50PF TPD0	3.2	3.3	3.5	3.3	3.3	3.6	3.4	3.4	3.7
2A-2Y 150PF TPD1	3.1	3.7	5.3	3.2	3.9	5.6	3.2	4.2	6.1
2A-2Y 150PF TPD0	5.1	5.3	5.6	5.2	5.9	6.3	5.3	6.7	7.2
3A-3Y 250PF TPD1	3.9	4.5	6.6	4.0	4.6	6.8	4.1	5.0	7.1
3A-3Y 250PF TPD0	6.4	6.4	6.8	6.5	6.6	7.0	6.8	6.9	7.2
4A-4Y 30X TPD1	1.2	1.0	3.0	1.3	1.9	3.2	1.7	2.4	3.5
4A-4Y 30X TPD0	2.0	2.0	2.2	2.4	2.3	2.4	2.5	2.5	2.5
T-RISE 50PF	1.1	1.2	1.5	1.1	1.2	1.5	1.1	1.3	1.6
T-FALL 50PF	2.0	2.3	2.5	2.1	2.3	2.6	2.2	2.4	2.7
Δ 30X-50PF TPD1	.6	.5	.5	1.0	1.0	.9	1.1	1.1	1.0
Δ 30X-50PF TPD0	.7	.9	1.1	.9	1.0	1.2	1.3	1.3	1.3



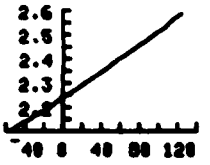
1A-1Y 50PF TPD1



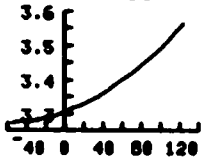
2A-2Y 150PF TPD0



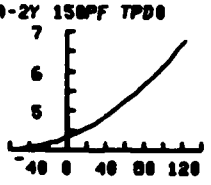
4A-4Y 30X TPD1



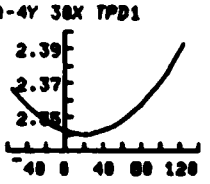
T-FALL 50PF



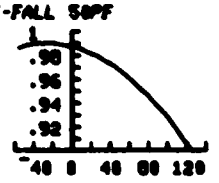
1A-1Y 50PF TPD0



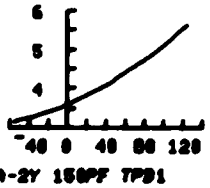
3A-3Y 250PF TPD1



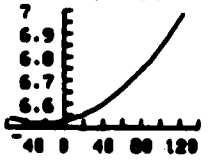
4A-4Y 30X TPD0



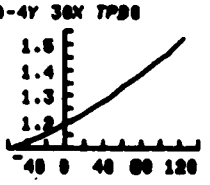
Δ 30X-50PF TPD1



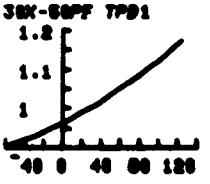
2A-2Y 150PF TPD1



3A-3Y 250PF TPD1



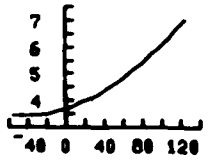
T-RISE 50PF



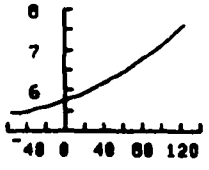
Δ 30X-50PF TPD0

CIRCUIT TYPE TEXAS INSTR. AS808 10/08/88 13:59:32

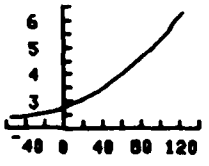
DELAY PATH	LOAD 50 PF 5.0 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	126 C	-55 C	25 C	125 C
1A-1Y 50PF TPD1	3.3	3.9	6.6	3.4	4.1	7.0	3.5	4.4	7.4
1A-1Y 50PF TPD0	3.5	4.1	5.7	4.1	4.4	6.1	5.5	4.0	6.6
2A-2Y 150PF TPD1	4.7	5.5	8.9	4.8	5.8	9.6	5.0	6.0	10.6
2A-2Y 150PF TPD0	5.3	5.8	7.3	5.4	6.0	7.6	5.5	6.1	7.9
3A-3Y 250PF TPD1	5.9	6.5	10.3	6.0	6.8	10.9	6.2	7.2	11.9
3A-3Y 250PF TPD0	6.5	7.0	8.5	7.0	7.3	8.9	7.1	7.4	9.2
4A-4Y 30X TPD1	2.2	2.9	5.7	2.4	3.2	6.3	2.5	3.7	7.0
4A-4Y 30X TPD0	2.2	2.8	4.3	2.7	3.1	4.0	3.5	3.5	5.2
T-RISE 50PF	1.2	1.2	1.6	1.3	1.3	1.6	1.3	1.3	1.6
T-FALL 50PF	2.0	2.2	2.5	2.2	2.3	2.5	2.9	2.4	2.6
Δ 30X-50PF TPD1	.9	.7	.3	1.0	.9	.7	1.2	1.1	1.1
Δ 30X-50PF TPD0	.6	.9	1.1	1.4	1.3	1.3	2.0	1.6	1.7



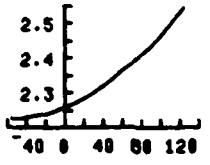
1A-1Y 50PF TPD1



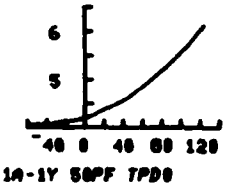
2A-2Y 150PF TPD0



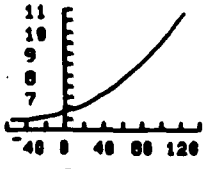
4A-4Y 30X TPD1



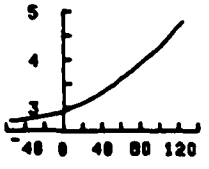
T-FALL 50PF



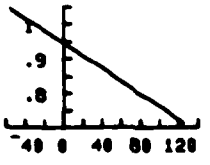
1A-1Y 50PF TPD0



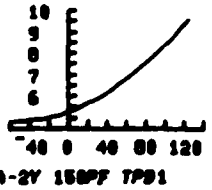
3A-3Y 250PF TPD1



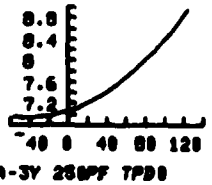
4A-4Y 30X TPD0



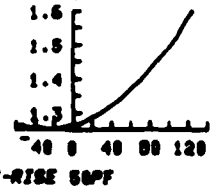
Δ 30X-50PF TPD1



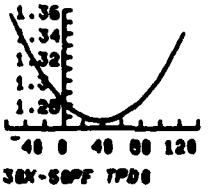
2A-2Y 150PF TPD1



3A-3Y 250PF TPD0



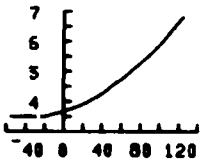
T-RISE 50PF



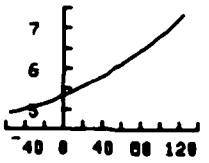
Δ 30X-50PF TPD0

CIRCUIT TYPE TEXAS INSTR. AS808 10/08/80 13:57:51

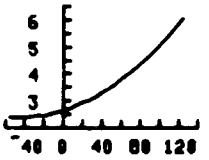
DELAY PATH	LOAD 50 PF 4.5 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
1A-1Y 50PF TPD1	3.4	3.8	6.4	3.5	4.0	6.8	3.6	4.3	7.2
1A-1Y 50PF TPD0	3.4	3.8	5.5	4.1	4.3	6.8	5.6	4.8	6.5
2A-2Y 150PF TPD1	5.2	5.7	8.7	5.2	5.9	9.5	5.3	7.2	10.5
2A-2Y 150PF TPD0	4.7	5.5	7.8	4.9	5.6	7.3	5.0	5.7	7.6
3A-3Y 250PF TPD1	6.3	6.7	10.1	6.4	7.0	10.7	6.6	7.3	11.8
3A-3Y 250PF TPD0	5.8	6.6	8.2	6.3	6.8	8.7	6.6	7.0	9.0
4A-4Y 30X TPD1	2.3	2.8	5.4	2.4	3.0	6.0	2.6	3.4	6.7
4A-4Y 30X TPD0	2.3	2.7	4.3	2.9	3.1	4.7	3.0	3.5	5.2
T-RISE 50PF	1.3	1.3	1.6	1.3	1.4	1.7	1.4	1.4	1.8
T-FALL 50PF	1.8	2.0	2.3	2.0	2.1	2.4	2.0	2.2	2.6
▲ 30X-50PF TPD1	.9	.8	.4	1.1	1.0	.8	1.3	1.1	1.1
▲ 30X-50PF TPD0	.3	.7	.9	1.2	1.2	1.2	1.0	1.7	1.6



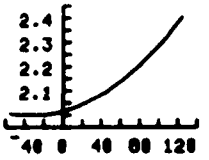
1A-1Y 50PF TPD1



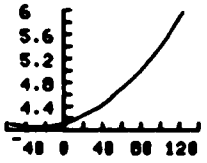
2A-2Y 150PF TPD0



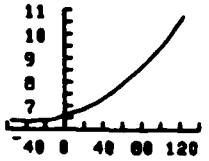
4A-4Y 30X TPD1



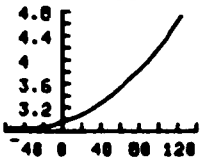
T-FALL 50PF



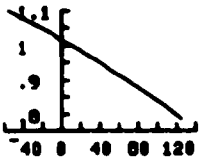
1A-1Y 50PF TPD0



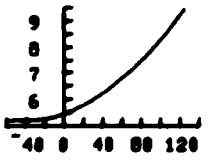
3A-3Y 250PF TPD1



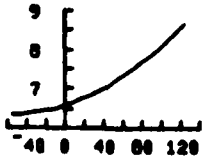
4A-4Y 30X TPD0



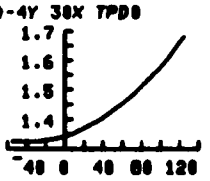
▲ 30X-50PF TPD1



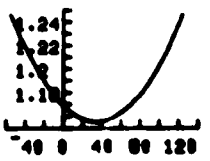
2A-2Y 150PF TPD1



3A-3Y 250PF TPD0



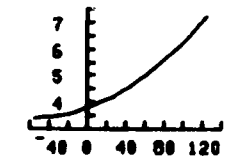
T-RISE 50PF



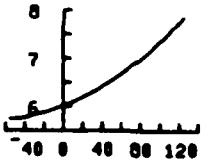
▲ 30X-50PF TPD0

CIRCUIT TYPE TEXAS INSTR. AS808 10/08/80 14:01:11

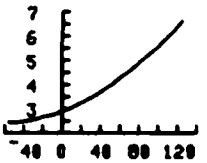
DELAY PATH	LOAD 50 PF 5.5 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
1A-1Y 50PF TPD1	3.3	4.0	6.0	3.4	4.2	7.2	3.5	4.6	7.6
1A-1Y 50PF TPD0	3.7	4.3	5.0	4.1	4.5	6.3	4.9	4.8	6.7
2A-2Y 150PF TPD1	4.5	5.5	9.1	4.6	5.8	9.8	4.8	6.6	10.6
2A-2Y 150PF TPD0	5.6	6.1	7.6	5.7	6.2	7.8	5.8	6.3	8.1
3A-3Y 250PF TPD1	5.6	6.5	10.4	5.8	6.8	11.0	6.0	7.2	12.1
3A-3Y 250PF TPD0	6.9	7.3	8.8	7.1	7.5	9.2	7.2	7.7	9.5
4A-4Y 30X TPD1	2.3	3.0	5.9	2.4	3.4	6.6	2.6	3.9	7.4
4A-4Y 30X TPD0	2.3	2.0	4.5	2.6	3.2	5.0	3.1	3.5	5.4
T-RISE 50PF	1.1	1.2	1.5	1.2	1.2	1.6	1.2	1.3	1.7
T-FALL 50PF	2.2	2.4	2.6	2.4	2.5	2.7	2.6	2.5	2.7
Δ 30X-50PF TPD1	.9	.6	.1	1.0	.0	.6	1.1	1.0	1.0
Δ 30X-50PF TPD0	1.0	1.0	1.0	1.4	1.3	1.3	1.0	1.7	1.0



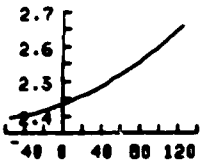
1A-1Y 50PF TPD1



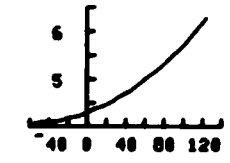
2A-2Y 150PF TPD0



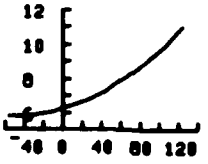
4A-4Y 30X TPD1



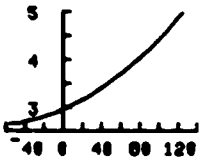
T-FALL 50PF



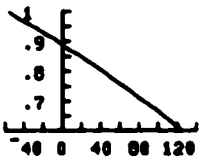
1A-1Y 50PF TPD0



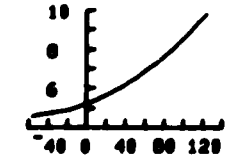
3A-3Y 250PF TPD1



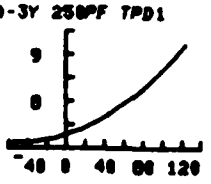
4A-4Y 30X TPD0



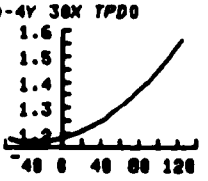
Δ 30X-50PF TPD1



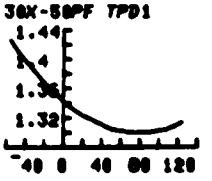
2A-2Y 150PF TPD1



3A-3Y 250PF TPD0

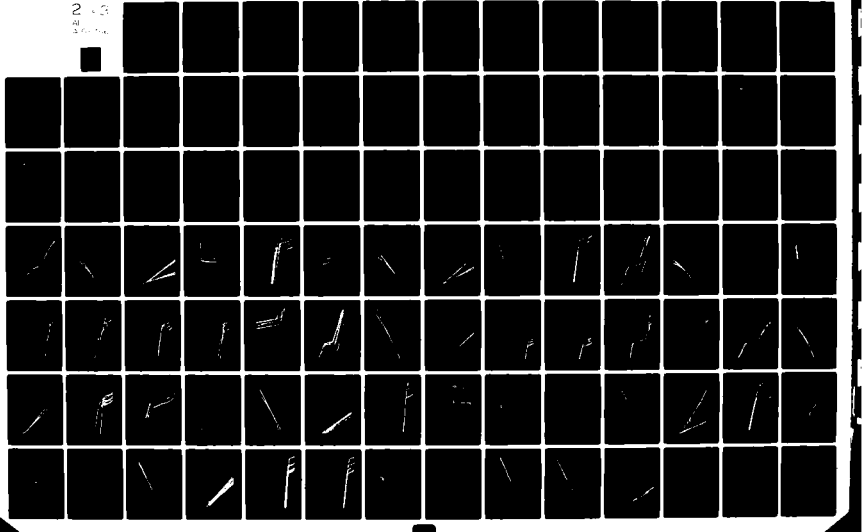


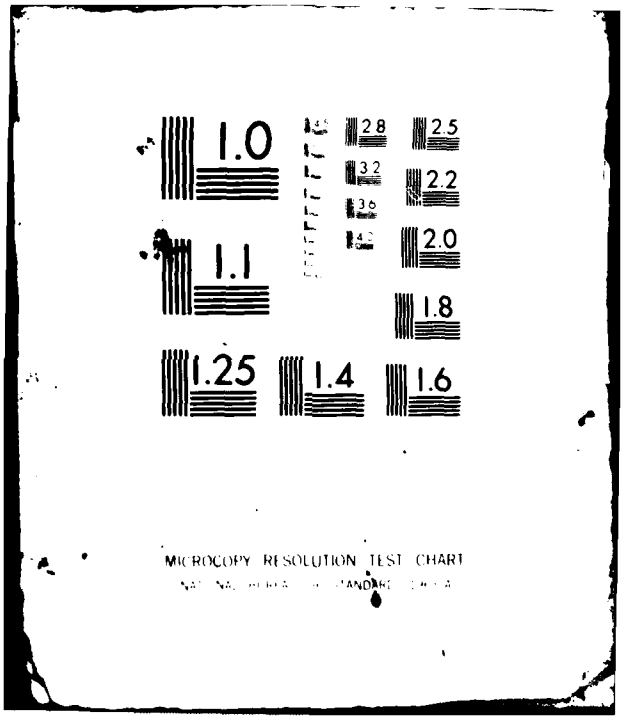
T-RISE 50PF



Δ 30X-50PF TPD0

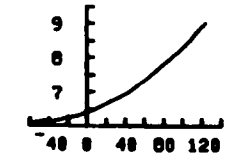
AD-A108 766 IBM FEDERAL SYSTEMS DIV MANASSAS VA F/G 9/1
ELECTRICAL CHARACTERIZATION OF SUPER SCHOTTKY.(U)
JUL 81 R A LAWRENCE F30602-80-C-0068
UNCLASSIFIED RADC-TR-81-194 NL



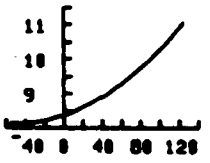

1.0
1.1
1.25
1.4
1.6
2.8
3.2
3.6
2.5
2.2
2.0
1.8
MICROCOPY RESOLUTION TEST CHART

CIRCUIT TYPE TEXAS INSTR. ADVANCED SCHOTTKY 181 SUM MODE SBPF 9/29/88 13:54:48

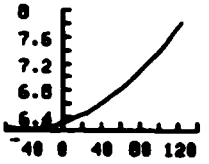
DELAY PATH	LOAD 50 PF 5.0 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
B0-F0 TPD1	6.1	6.6	6.5	6.1	6.7	9.0	6.2	6.9	12.1
B0-F0 TPD0 OP	9.6	10.6	10.6	9.0	10.0	13.4	10.0	11.1	14.2
B0-F3 TPD1 OP	6.8	7.4	7.4	7.0	7.6	10.2	7.2	7.9	10.9
B0-F3 TPD0 OP	8.0	8.5	8.5	8.1	8.7	11.0	8.3	8.9	11.7
B0-P TPD1 IP	4.8	5.2	5.2	4.9	5.3	6.7	4.9	5.4	7.2
B0-P TPD0 IP	6.4	6.8	6.9	6.5	6.9	8.3	6.7	7.1	9.3
B1-G TPD1 IP	6.2	6.3	6.3	6.2	6.5	7.8	6.3	6.6	8.3
B1-G TPD0 IP	5.3	5.8	5.9	5.4	6.0	7.5	5.6	6.2	8.0
B1-CN+4 TPD1 OP	8.8	9.5	9.6	8.9	9.8	12.3	9.1	10.2	12.9
B1-CN+4 TPD0 OP	8.7	8.9	9.0	8.9	9.2	12.0	9.0	9.4	12.0
CN-F3 TPD1 IP	5.1	5.2	5.2	5.1	5.4	7.3	5.3	5.6	7.8
CN-F3 TPD0 IP	5.9	6.3	6.4	6.0	6.5	8.1	6.2	6.7	8.7
CN-CN+4 TPD1 IP	6.3	6.2	6.4	6.5	6.5	8.0	6.6	6.7	8.6
CN-CN+4 TPD0 IP	4.5	5.3	5.4	4.6	5.5	7.3	4.7	5.8	7.8



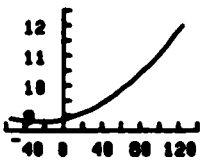
B0-F0 TPD1



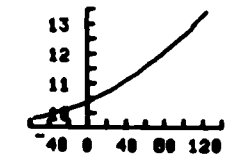
B0-F3 TPD0 OP



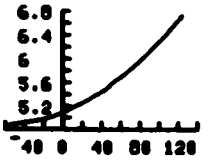
B1-G TPD1 IP



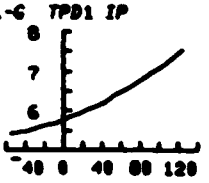
B1-CN+4 TPD0 OP



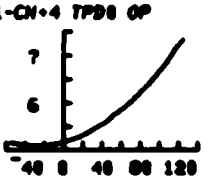
B0-F0 TPD0 OP



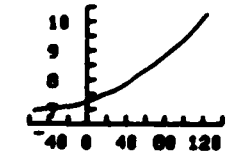
B0-P TPD1 IP



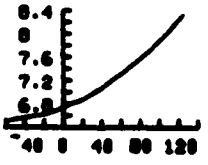
B1-G TPD0 IP



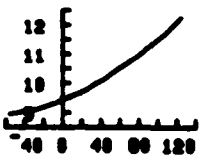
CN-F3 TPD1 IP



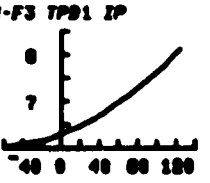
B0-F3 TPD1 OP



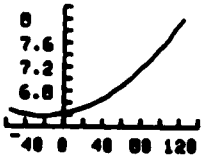
B0-P TPD0 IP



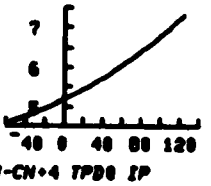
B1-CN+4 TPD1 OP



CN-F3 TPD0 IP



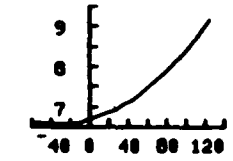
CN-CN+4 TPD1 IP



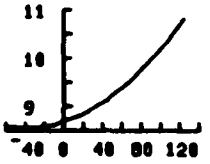
CN-CN+4 TPD0 IP

CIRCUIT TYPE TEXAS INSTR. ADVANCED SCHOTTKY 181 SUM MODE 50PF 9/29/80 13:52:48

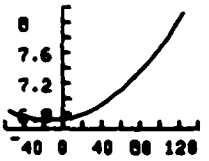
DELAY PATH	LOAD 50 PF 4.5 VOLTS MINIMUM -55 C	25 C	125 C	AVERAGE -55 C	25 C	125 C	MAXIMUM -55 C	25 C	125 C
B0-F0 TPD1	6.6	6.8	8.6	6.6	6.9	9.2	6.7	7.1	11.1
B0-F0 TPD0 OP	9.9	10.7	12.9	10.0	10.9	13.4	10.2	11.2	14.0
B0-F3 TPD1 OP	7.2	7.6	10.0	7.4	7.8	10.5	7.6	8.0	10.9
B0-F3 TPD0 OP	8.5	8.8	10.4	8.6	8.9	10.8	8.7	9.1	11.2
B0-P TPD1 IP	5.3	5.4	6.8	5.3	5.5	7.1	5.4	5.6	7.4
B0-P TPD0 IP	6.5	7.0	8.0	6.7	7.1	8.2	6.9	7.2	8.7
B1-G TPD1 IP	6.8	6.7	7.9	6.8	6.8	8.1	6.9	7.0	8.4
B1-G TPD0 IP	5.4	5.7	7.2	5.4	5.8	7.5	5.5	6.0	7.7
B1-CN+4 TPD1 OP	9.3	9.7	12.1	9.4	10.0	12.5	9.5	10.2	13.1
B1-CN+4 TPD0 OP	9.3	9.2	11.2	9.4	9.4	11.7	9.5	9.6	12.3
CN-F3 TPD1 IP	5.5	5.6	7.1	5.7	5.7	7.4	5.8	5.9	7.8
CN-F3 TPD0 IP	6.0	6.4	7.6	6.2	6.5	7.9	6.3	6.7	8.2
CN-CN+4 TPD1 IP	7.0	6.8	7.6	7.2	7.1	8.3	7.3	7.2	8.7
CN-CN+4 TPD0 IP	4.4	4.9	6.7	4.5	5.1	7.0	4.6	5.3	7.3



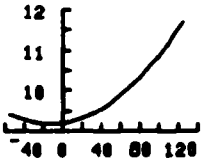
B0-F0 TPD1



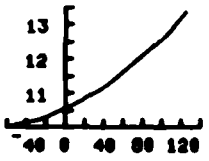
B0-F3 TPD0 OP



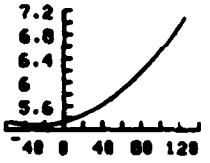
B1-G TPD1 IP



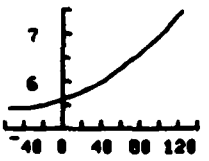
B1-CN+4 TPD0 OP



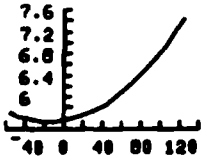
B0-F0 TPD0 OP



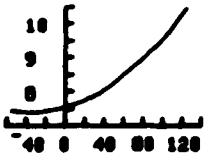
B0-P TPD1 IP



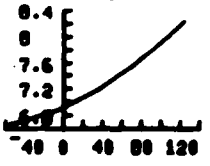
B1-G TPD0 IP



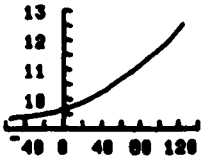
CN-F3 TPD1 IP



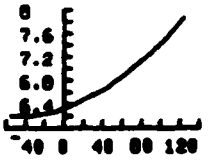
B0-F3 TPD1 OP



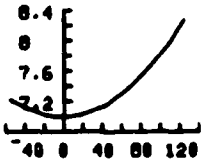
B0-P TPD0 IP



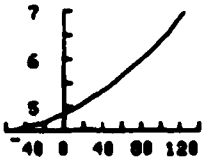
B1-CN+4 TPD1 OP



CN-F3 TPD0 IP



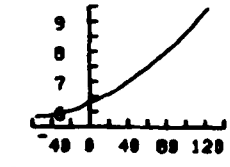
CN-CN+4 TPD1 IP



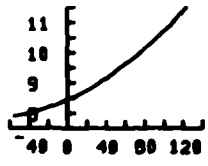
CN-CN+4 TPD0 IP

CIRCUIT TYPE TEXAS INSTR. ADVANCED SCHOTTKY 181 SUM MODE 50PF 9/29/88 13:56:31

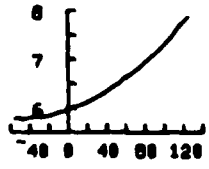
DELAY PATH	LOAD 50 PF 5.5 VOLTS MINIMUM -55 C	25 C	125 C	AVERAGE -55 C	25 C	125 C	MAXIMUM -55 C	25 C	125 C
B0-F0 TPD1	5.8	6.6	8.7	5.8	6.7	9.5	5.9	6.9	12.8
B0-F0 TPD0 OP	9.6	10.6	13.4	9.8	10.8	13.8	9.9	11.1	14.4
B0-F3 TPD1 OP	6.4	7.4	10.2	6.6	7.7	10.7	6.8	8.0	11.1
B0-F3 TPD0 OP	7.8	8.6	11.2	7.9	8.9	11.5	8.0	9.1	11.9
B0-P TPD1 IP	4.5	4.9	6.5	4.6	5.1	6.8	4.6	5.2	7.1
B0-P TPD0 IP	6.3	6.8	8.4	6.5	7.0	8.6	6.7	7.1	9.9
B1-G TPD1 IP	5.7	6.0	7.7	5.8	6.2	7.9	5.9	6.4	8.2
B1-G TPD0 IP	5.3	6.1	7.5	5.5	6.3	7.8	5.6	6.5	8.0
B1-CN+4 TPD1 OP	8.5	9.6	12.0	8.7	9.9	12.5	8.9	10.3	13.0
B1-CN+4 TPD0 OP	8.4	8.9	12.0	8.6	9.3	12.6	8.7	9.6	13.0
CN-F3 TPD1 IP	4.7	5.2	7.5	4.8	5.4	7.8	4.9	5.6	8.2
CN-F3 TPD0 IP	5.8	6.5	8.3	5.9	6.7	8.6	6.1	6.9	9.0
CN-CN+4 TPD1 IP	5.7	5.8	7.5	5.9	6.2	8.1	6.0	6.4	8.5
CN-CN+4 TPD0 IP	4.8	5.7	7.4	4.9	6.0	7.8	5.0	6.3	8.2



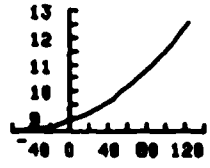
B0-F0 TPD1



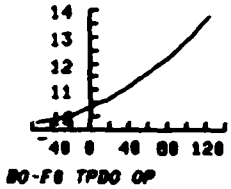
B0-F3 TPD0 OP



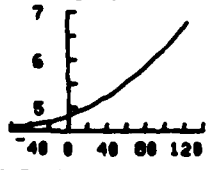
B1-G TPD1 IP



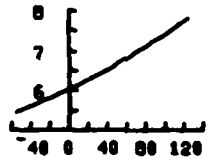
B1-CN+4 TPD0 OP



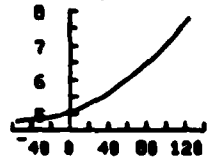
B0-F0 TPD0 OP



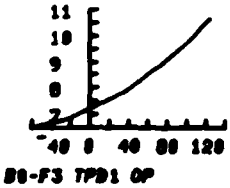
B0-P TPD1 IP



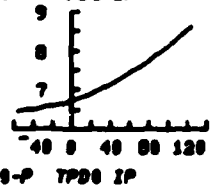
B1-G TPD0 IP



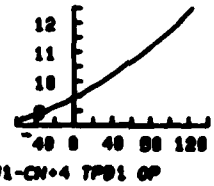
CN-F3 TPD1 IP



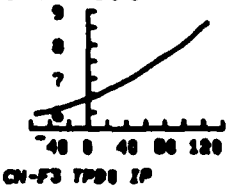
B0-F3 TPD1 OP



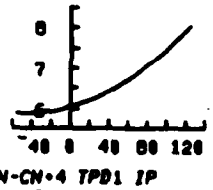
B0-P TPD0 IP



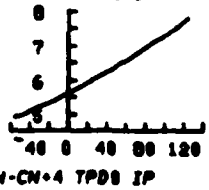
B1-CN+4 TPD1 OP



CN-F3 TPD0 IP



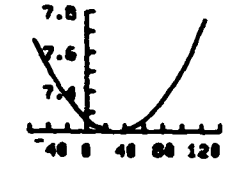
CN-CN+4 TPD1 IP



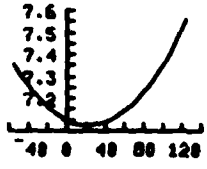
CN-CN+4 TPD0 IP

CIRCUIT TYPE FAIRCHILD FAST 101 SUM MODE SOFT 9/29/88 11:49:07

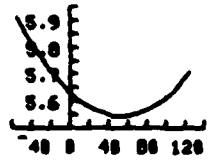
DELAY PATH	LOAD	SS MINIMUM		PF	S.S VOLTS AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
B0-F0 TPD1 IP	7.2	6.9	7.2	7.7	7.2	7.8	7.9	7.3	8.5
B0-F0 TPD0 OP	7.3	6.9	7.6	7.4	7.2	7.9	8.1	7.8	8.1
B0-F3 TPD1 OP	7.8	7.2	8.6	8.0	7.8	9.6	8.1	8.8	10.6
B0-F3 TPD0 OP	7.1	6.7	7.3	7.4	7.1	7.6	8.1	7.4	7.8
B0-P TPD1 IP	5.2	4.8	5.8	5.3	4.9	5.3	5.4	5.8	5.6
B0-P TPD0 IP	5.2	5.1	5.9	5.3	5.4	6.2	5.4	5.6	6.5
B1-G TPD1 IP	5.8	5.4	5.5	5.9	5.6	5.7	6.8	5.7	5.9
B1-G TPD0 IP	4.7	5.8	5.5	4.8	5.1	5.9	4.9	5.5	6.2
B1-CN+4 TPD1 OP	9.4	9.2	9.9	9.6	9.5	10.8	9.8	10.1	11.6
B1-CN+4 TPD0 OP	9.2	8.7	8.8	9.4	8.9	8.9	9.5	9.2	9.1
CN-F3 TPD1 IP	6.8	5.7	6.2	6.1	5.8	6.7	6.2	6.9	7.1
CN-F3 TPD0 IP	5.8	5.8	6.8	5.2	5.3	6.3	6.1	5.8	6.5
CN-CN+4 TPD1 IP	5.4	4.2	5.6	5.4	5.2	6.2	5.6	5.3	6.7
CN-CN+4 TPD0 IP	4.9	4.7	4.9	5.0	4.9	5.1	5.1	6.5	5.2



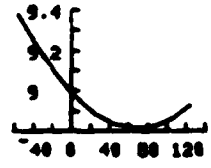
B0-F0 TPD1



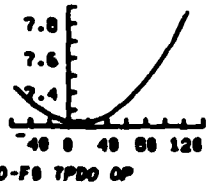
B0-F3 TPD0 OP



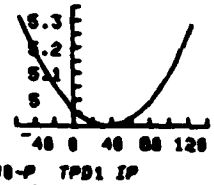
B1-G TPD1 IP



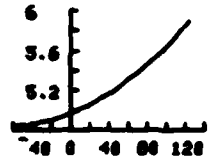
B1-CN+4 TPD0 OP



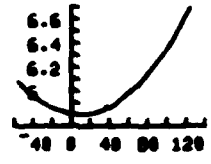
B0-F0 TPD0 OP



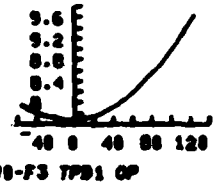
B0-P TPD1 IP



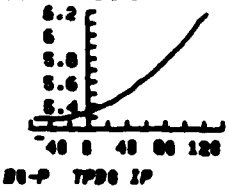
B1-G TPD0 IP



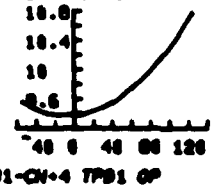
CN-F3 TPD1 IP



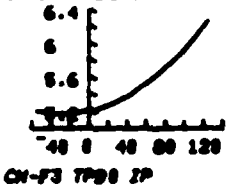
B0-F3 TPD1 OP



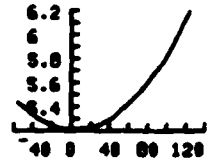
B0-P TPD0 IP



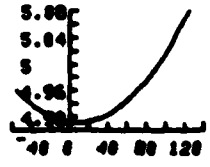
B1-CN+4 TPD1 OP



CN-F3 TPD0 IP



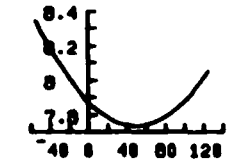
CN-CN+4 TPD1 IP



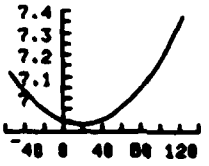
CN-CN+4 TPD0 IP

CIRCUIT TYPE FAIRCHILD FAST 181 SUM MODE 50PF 9/29/80 11:48:03

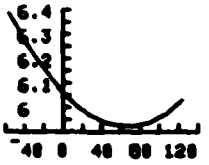
DELAY PATH	LOAD 50 PF 4.5 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
B0-F0 TPD1	7.8	7.4	7.5	8.4	7.8	8.1	8.6	7.9	8.5
B0-F0 TPD0 OP	7.2	6.7	7.4	7.3	7.1	7.7	7.7	7.3	7.9
B0-F3 TPD1 OP	8.8	8.3	9.2	9.0	8.7	10.0	9.1	8.9	10.8
B0-F3 TPD0 OP	6.8	6.6	7.1	7.1	6.9	7.4	8.8	7.2	7.6
B0-P TPD1 IP	5.7	5.2	5.2	5.8	5.3	5.5	5.8	5.4	5.8
B0-P TPD0 IP	5.2	5.2	6.8	5.3	5.5	6.3	5.4	5.7	6.5
B1-G TPD1 IP	6.3	5.8	5.9	6.4	6.0	6.0	6.5	6.1	6.2
B1-G TPD0 IP	4.7	5.8	5.6	4.8	5.1	5.9	4.9	5.8	6.2
B1-CN+4 TPD1 OP	10.1	10.0	10.6	10.3	10.3	11.2	10.5	11.0	11.8
B1-CN+4 TPD0 OP	9.6	9.0	9.8	9.7	9.2	9.1	9.8	9.5	9.2
CN-F3 TPD1 IP	6.6	6.1	6.4	6.8	6.3	6.9	7.0	6.4	7.2
CN-F3 TPD0 IP	4.9	4.8	5.7	5.0	5.1	6.1	6.0	5.6	6.3
CN-CN+4 TPD1 IP	5.9	4.9	6.8	6.0	5.7	6.5	6.1	5.9	6.9
CN-CN+4 TPD0 IP	5.1	4.8	5.8	5.1	5.0	5.2	5.2	6.5	5.3



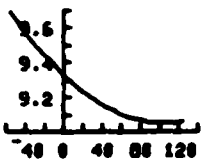
B0-F0 TPD1



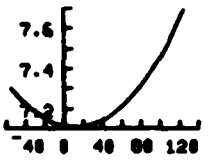
B0-F3 TPD0 OP



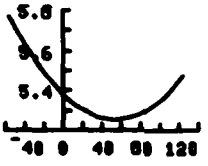
B1-G TPD1 IP



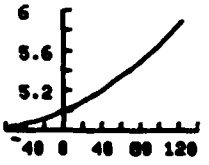
B1-CN+4 TPD0 OP



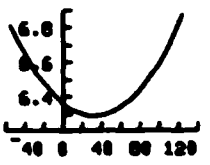
B0-F0 TPD0 OP



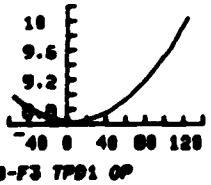
B0-P TPD1 IP



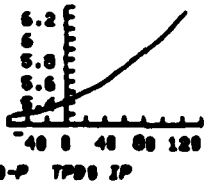
B1-G TPD0 IP



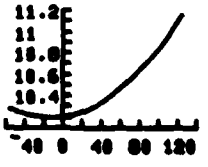
CN-F3 TPD1 IP



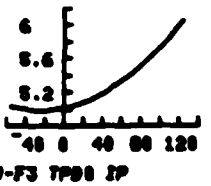
B0-F3 TPD1 OP



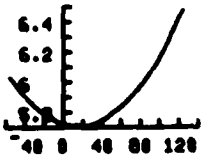
B0-P TPD0 IP



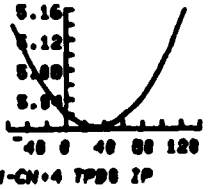
B1-CN+4 TPD1 OP



CN-F3 TPD0 IP



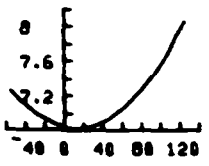
CN-CN+4 TPD1 IP



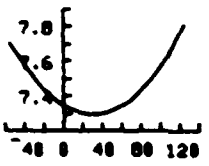
CN-CN+4 TPD0 IP

CIRCUIT TYPE FAIRCHILD FAST 181 SUM MODE 50PF 9/29/88 11:51:52

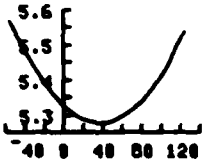
DELAY PATH	LOAD	50	PF	5.5	VOLTS				
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
B0-F0 TPD1	6.9	6.5	7.2	7.3	6.8	8.1	7.5	7.0	9.3
B0-F0 TPD0 OP	7.3	7.0	7.8	7.7	7.4	8.8	8.2	7.6	8.2
B0-F3 TPD1 OP	7.8	6.5	8.5	7.1	7.1	9.7	7.3	7.3	10.8
B0-F3 TPD0 OP	7.5	6.9	7.6	7.7	7.3	7.8	8.8	7.6	8.8
B0-P TPD1 IP	4.9	4.5	4.9	5.0	4.6	5.2	5.0	4.8	5.7
B0-P TPD0 IP	5.1	5.0	5.9	5.2	5.4	6.3	5.4	5.5	6.6
B1-G TPD1 IP	5.5	5.0	5.3	5.6	5.3	5.5	5.7	5.4	5.8
B1-G TPD0 IP	4.7	4.9	5.7	4.8	5.1	6.0	5.0	5.4	6.4
B1-CN+4 TPD1 OP	8.0	8.7	9.0	9.1	8.9	10.0	9.3	9.3	11.6
B1-CN+4 TPD0 OP	9.0	8.5	8.7	9.1	8.7	8.9	9.3	8.9	9.1
CN-F3 TPD1 IP	5.6	5.3	6.1	5.6	5.5	6.7	5.7	5.5	7.1
CN-F3 TPD0 IP	5.4	5.3	6.3	5.6	5.6	6.5	6.1	5.9	6.8
CN-CN+4 TPD1 IP	4.9	3.8	5.6	5.0	4.9	6.2	5.1	5.0	6.6
CN-CN+4 TPD0 IP	4.8	4.6	4.9	4.9	4.8	5.1	5.1	6.5	5.2



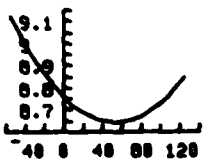
B0-F0 TPD1



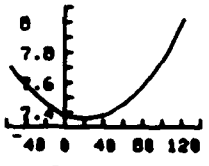
B0-F3 TPD0 OP



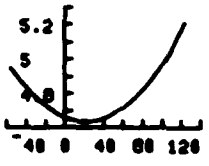
B1-G TPD1 IP



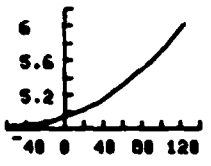
B1-CN+4 TPD0 OP



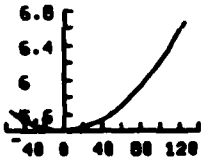
B0-F0 TPD0 OP



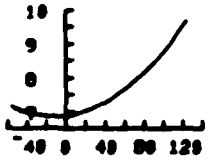
B0-P TPD1 IP



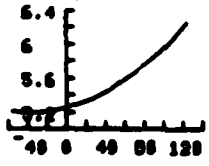
B1-G TPD0 IP



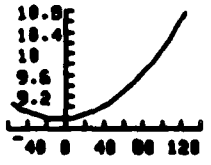
CN-F3 TPD1 IP



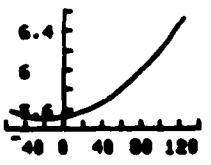
B0-F3 TPD1 OP



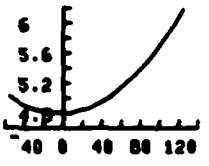
B0-P TPD0 IP



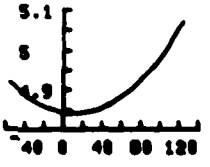
B1-CN+4 TPD1 OP



CN-F3 TPD0 IP



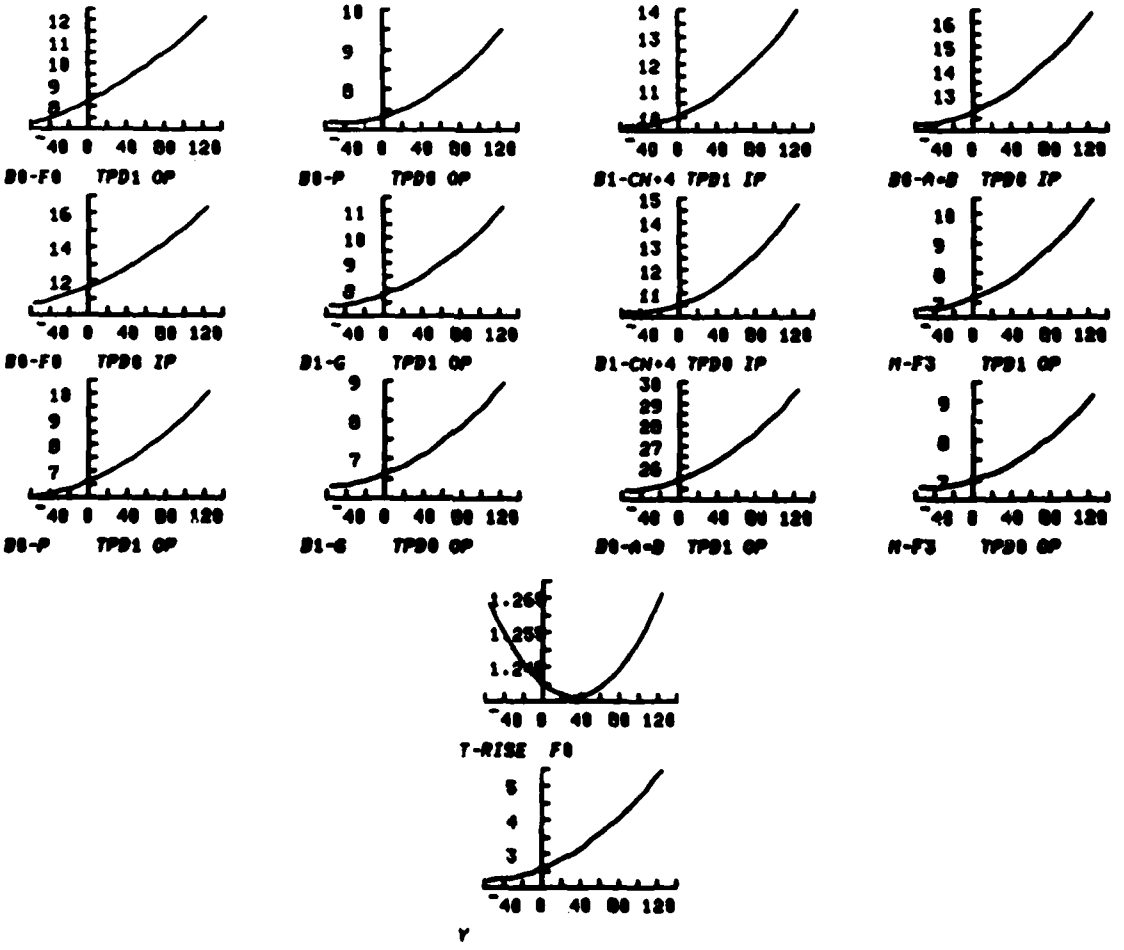
CN-CN+4 TPD1 IP



CN-CN+4 TPD0 IP

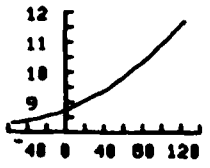
CIRCUIT TYPE TEXAS INSTR. ADVANCED SCHOTTKY 181 DIFF MODE 50PF 9/29/86 13:27:53

DELAY PATH		LOAD 50 PF 5.0 VOLTS								
		MINIMUM			AVERAGE			MAXIMUM		
		-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
B0-F0	TPD1 OP	2.6	8.7	11.8	7.3	8.9	12.2	7.9	9.1	12.6
B0-F0	TPD0 IP	10.6	12.8	16.1	10.7	12.3	16.4	10.9	12.8	17.1
B0-P	TPD1 OP	6.8	6.8	9.8	6.1	7.1	10.8	6.2	7.5	10.4
B0-P	TPD0 OP	7.1	7.4	9.3	7.2	7.6	9.5	7.4	7.7	9.8
B1-G	TPD1 OP	7.3	8.8	11.8	7.4	8.2	11.2	7.5	8.5	11.5
B1-G	TPD0 OP	6.2	6.7	8.7	6.3	6.9	9.8	6.4	7.2	9.2
B1-CN+4	TPD1 IP	9.6	10.3	13.6	9.7	10.5	14.8	9.8	10.8	14.5
B1-CN+4	TPD0 IP	10.1	10.6	14.5	10.2	10.9	14.8	10.4	11.4	15.3
B0-A+B	TPD1 OP	24.7	25.7	29.4	24.9	26.9	29.7	25.1	26.4	30.0
B0-A+B	TPD0 IP	11.6	12.5	16.0	11.7	12.8	16.4	11.9	13.2	16.9
M-F3	TPD1 OP	6.6	7.2	10.3	6.8	7.5	10.4	6.9	7.9	10.8
M-F3	TPD0 OP	6.7	7.0	8.9	6.8	7.2	9.2	6.9	7.4	9.4
T-RISE	F0	1.2	1.2	1.2	1.3	1.2	1.3	1.3	1.3	1.3
Y		2.2	2.8	5.4	2.2	2.9	5.5	2.3	3.1	5.7

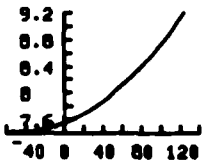


CIRCUIT TYPE TEXAS INSTR. ADVANCED SCHOTTKY 181 DIFF MODE 50PF 9/29/88 13:26:59

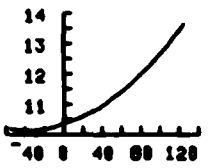
DELAY PATH		LOAD 50 PF 4.5 VOLTS MINIMUM -55 C	25 C	125 C	AVERAGE -55 C	25 C	125 C	MAXIMUM -55 C	25 C	125 C
B0-F0	TPD1 OP	8.2	8.9	11.4	8.3	9.1	11.7	8.4	9.4	12.1
B0-F0	TPD0 IP	11.8	12.1	15.7	11.1	12.4	16.0	11.3	12.7	16.0
B0-P	TPD1 OP	6.4	7.1	9.6	6.5	7.2	9.9	6.6	7.4	10.3
B0-P	TPD0 OP	7.3	7.6	9.0	7.4	7.7	9.2	7.6	7.8	9.3
B1-G	TPD1 OP	8.0	8.4	10.7	8.0	8.5	11.0	8.1	8.8	11.5
B1-G	TPD0 OP	6.3	6.6	8.5	6.3	6.7	8.7	6.5	6.8	8.8
B1-CN+4	TPD1 IP	10.1	10.5	13.4	10.2	10.7	13.6	10.3	10.9	14.1
B1-CN+4	TPD0 IP	10.6	10.9	13.8	10.7	11.1	14.1	10.9	11.4	14.7
B0-A+B	TPD1 OP	27.9	28.5	31.6	28.2	28.7	31.9	28.5	29.0	32.4
B0-A+B	TPD0 IP	12.2	12.7	15.6	12.3	13.0	16.0	12.5	13.3	16.6
M-F3	TPD1 OP	7.4	7.5	10.1	7.6	7.7	10.4	7.8	8.0	10.8
M-F3	TPD0 OP	6.9	7.1	8.6	7.0	7.2	8.8	7.1	7.4	9.0
T-RISE	F0	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.4
Y		1.9	2.4	4.9	2.0	2.6	5.0	2.0	2.0	5.2



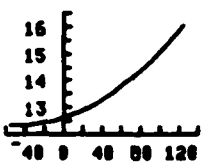
B0-F0 TPD1 OP



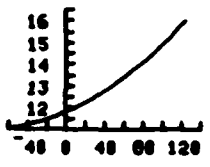
B0-P TPD0 OP



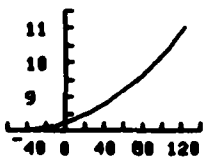
B1-CN+4 TPD1 IP



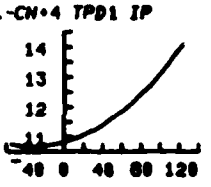
B0-A+B TPD0 IP



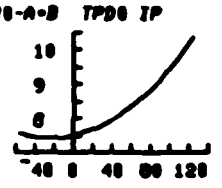
B0-F0 TPD0 IP



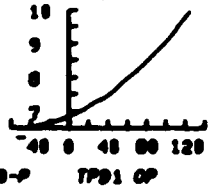
B1-G TPD1 OP



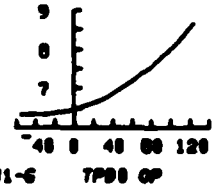
B1-CN+4 TPD0 IP



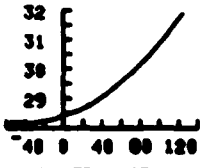
M-F3 TPD1 OP



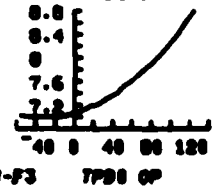
B0-P TPD1 OP



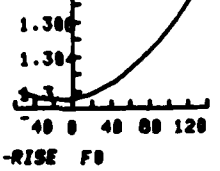
B1-G TPD0 OP



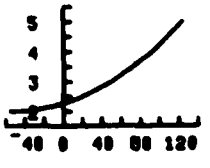
B0-A+B TPD1 OP



M-F3 TPD0 OP



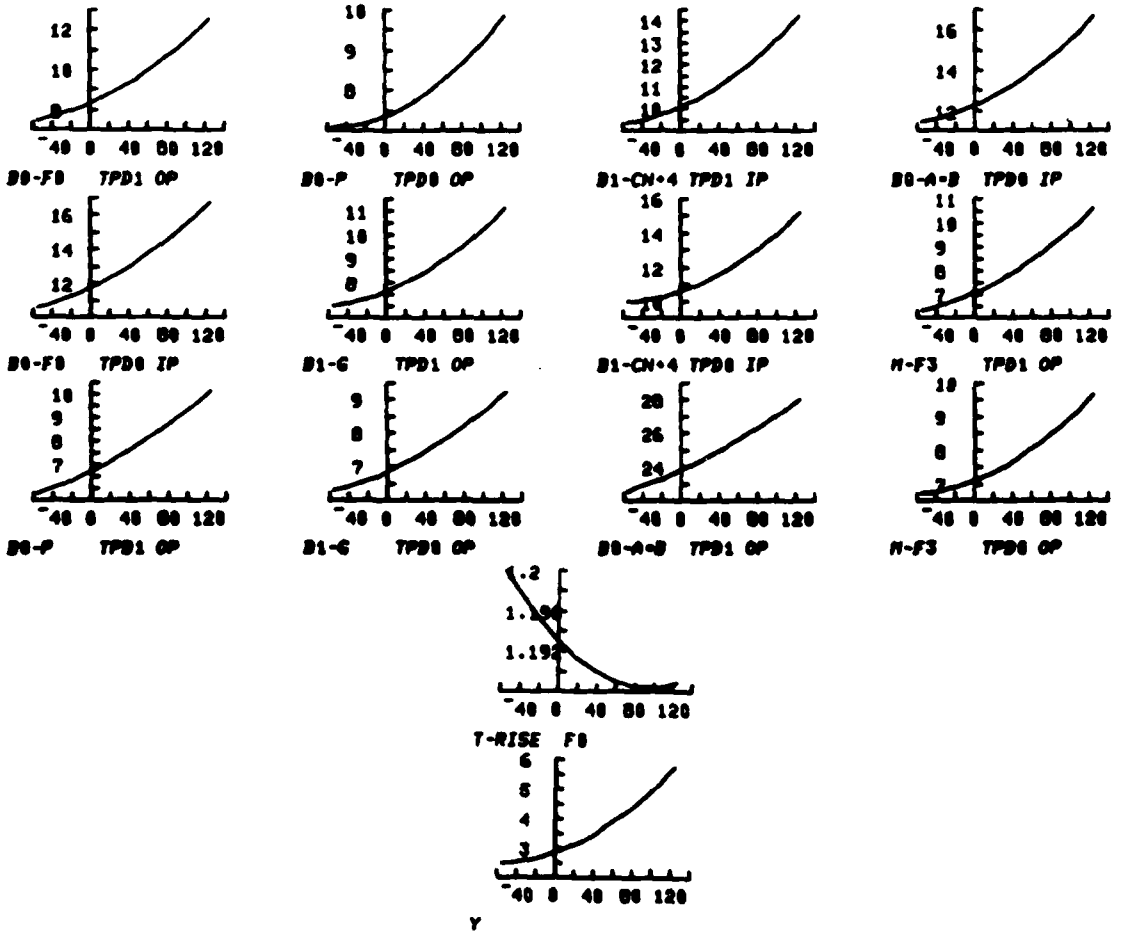
T-RISE F0



Y

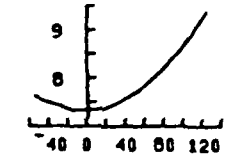
CIRCUIT TYPE TEXAS INSTR. ADVANCED SCHOTTKY 101 DIFF MODE 50PF 9/29/88 13:29:47

DELAY PATH		LOAD 50 PF 5.5 VOLTS								
		MINIMUM			AVERAGE			MAXIMUM		
		-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
B0-F0	TPD1 OP	7.4	8.6	12.2	7.5	8.9	12.5	7.6	9.2	12.9
B0-F0	TPD0 IP	10.5	12.2	16.4	10.6	12.5	16.8	10.8	13.1	17.4
B0-P	TPD1 OP	5.7	7.0	9.9	5.8	7.3	10.1	5.9	7.7	10.5
B0-P	TPD0 OP	7.0	7.5	9.7	7.1	7.6	9.9	7.2	7.9	10.0
B1-G	TPD1 OP	6.9	7.0	10.9	7.0	8.1	11.1	7.1	8.5	11.5
B1-G	TPD0 OP	6.2	6.8	9.0	6.3	7.2	9.3	6.4	7.5	9.5
B1-CN+4	TPD1 IP	9.2	10.2	13.9	9.4	10.6	14.2	9.5	11.1	14.0
B1-CN+4	TPD0 IP	9.0	10.7	14.9	9.9	11.1	15.2	10.2	11.7	15.0
B0-A+B	TPD1 OP	22.4	23.9	27.0	22.6	24.5	28.1	22.6	28.0	28.4
B0-A+B	TPD0 IP	11.3	12.5	16.3	11.5	12.0	16.7	11.7	13.4	17.2
H-F3	TPD1 OP	6.1	7.3	10.3	6.3	7.6	10.6	6.5	8.0	11.1
H-F3	TPD0 OP	6.6	7.2	9.4	6.7	7.4	9.6	6.9	7.7	9.9
T-RISE	F0	1.2	1.1	1.1	1.2	1.2	1.2	1.2	1.3	1.2
Y		2.4	2.6	5.6	2.5	3.2	5.7	2.5	3.9	6.0

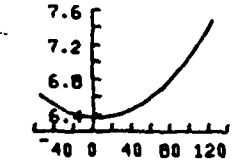


CIRCUIT TYPE FAIRCHILD FAST 181 DIFF MODE 50PF 10/01/80 8:40:30

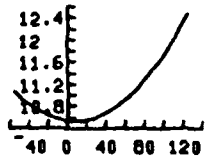
DELAY PATH		LOAD 50 PF 5.0 VOLTS MINIMUM -55 C	25 C	125 C	AVERAGE -55 C	25 C	125 C	MAXIMUM -55 C	25 C	125 C
B0-F0	TPD1 OP	7.2	7.0	8.9	7.6	7.4	9.4	7.8	7.7	10.2
B0-F0	TPD0 IP	7.8	7.4	9.1	8.0	7.9	9.6	8.4	8.1	10.0
B0-P	TPD1 OP	5.9	5.5	6.7	5.9	5.7	7.1	6.0	5.8	7.6
B0-P	TPD0 OP	6.5	6.0	7.1	6.6	6.4	7.5	6.8	6.5	7.8
B1-G	TPD1 OP	6.7	6.2	7.3	6.8	6.5	7.6	6.8	6.7	7.9
B1-G	TPD0 OP	6.2	6.1	7.0	6.3	6.3	7.4	6.4	6.7	7.7
B1-CN+4	TPD1 IP	10.8	10.3	11.7	11.1	10.6	12.5	11.3	11.1	13.1
B1-CN+4	TPD0 IP	10.1	9.5	10.5	10.3	9.8	10.7	10.4	10.1	11.1
B0-A+B	TPD1 OP	29.4	29.0	34.0	29.8	29.3	36.0	30.0	29.7	37.5
B0-A+B	TPD0 IP	9.7	8.8	10.2	9.9	9.3	10.6	10.1	9.4	11.0
M-F3	TPD1 OP	7.5	7.1	8.8	7.7	7.4	9.4	7.8	7.6	9.8
M-F3	TPD0 OP	6.5	6.2	6.9	6.7	6.4	7.2	7.6	6.6	7.5
T-RISE	F0	1.6	1.6	1.6	1.7	1.6	1.7	1.7	1.7	1.8
T-FALL	F0	2.1	2.1	2.3	2.2	2.2	2.3	2.8	2.4	2.4



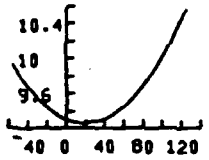
B0-F0 TPD1 OP



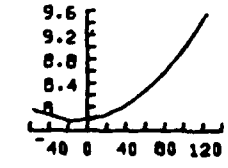
B0-P TPD0 OP



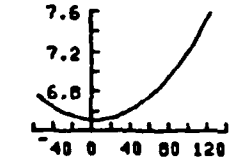
B1-CN+4 TPD1 IP



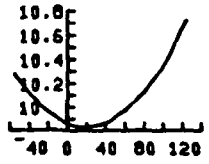
B0-A+B TPD0 IP



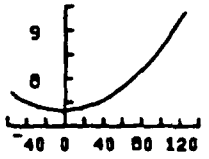
B0-F0 TPD0 IP



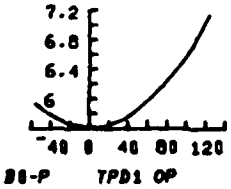
B1-G TPD1 OP



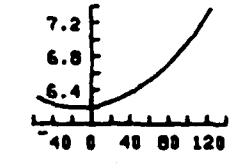
B1-CN+4 TPD0 IP



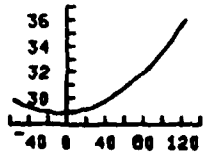
M-F3 TPD1 OP



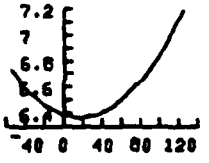
B0-P TPD1 OP



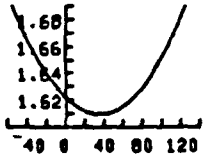
B1-G TPD0 OP



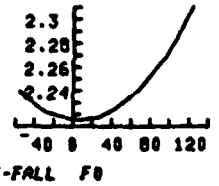
B0-A+B TPD1 OP



M-F3 TPD0 OP



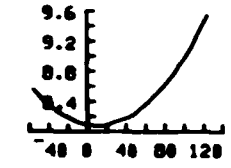
T-RISE F0



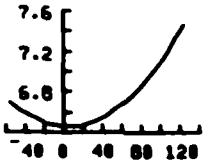
T-FALL F0

CIRCUIT TYPE FAIRCHILD FAST 181 DIFF MODE 50PF 10/01/80 8:38:38

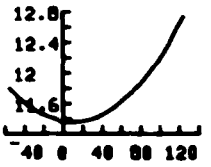
DELAY PATH		LOAD 50 PF 4.5 VOLTS MINIMUM -55 C	25 C	125 C	AVERAGE -55 C	25 C	125 C	MAXIMUM -55 C	25 C	125 C
B0-F0	TPD1 OP	8.0	7.7	9.2	8.6	8.1	9.5	8.8	8.3	10.1
B0-F0	TPD0 IP	7.9	7.4	9.1	8.2	8.0	9.4	8.6	8.2	9.7
B0-P	TPD1 OP	6.5	5.8	7.8	6.6	6.2	7.3	6.7	6.3	7.7
B0-P	TPD0 OP	6.6	6.2	7.2	6.7	6.5	7.5	6.8	6.6	7.8
B1-G	TPD1 OP	7.4	6.7	7.6	7.5	7.1	7.9	7.6	7.2	8.2
B1-G	TPD0 OP	6.2	6.2	7.1	6.3	6.3	7.3	6.4	7.8	7.6
B1-CN+4	TPD1 IP	11.6	11.1	12.2	11.8	11.4	12.7	11.9	12.2	13.3
B1-CN+4	TPD0 IP	10.7	9.8	10.7	10.8	10.3	10.9	10.9	10.6	11.1
B0-A-B	TPD1 OP	33.7	32.7	36.6	33.9	33.1	38.2	34.3	33.5	39.2
B0-A-B	TPD0 IP	10.5	9.1	10.3	10.7	9.7	10.6	10.9	9.9	10.9
M-F3	TPD1 OP	8.7	8.8	9.1	8.9	8.3	9.6	9.8	8.4	10.8
M-F3	TPD0 OP	6.3	6.1	6.6	6.5	6.3	6.9	7.2	6.6	7.2
T-RISE	F0	1.9	1.8	1.7	1.9	1.8	1.8	2.8	1.9	1.8
T-FALL	F0	1.9	1.9	2.2	2.8	2.1	2.3	2.8	2.4	2.3



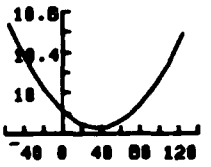
B0-F0 TPD1 OP



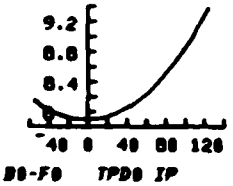
B0-P TPD0 OP



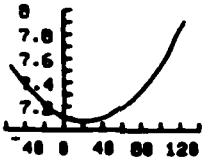
B1-CN+4 TPD1 IP



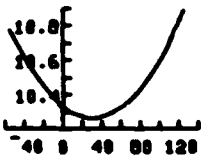
B0-A-B TPD0 IP



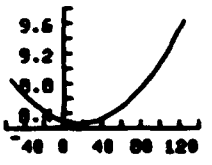
B0-F0 TPD0 IP



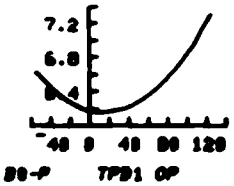
B1-G TPD1 OP



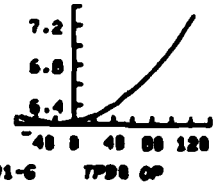
B1-CN+4 TPD0 IP



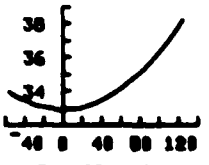
M-F3 TPD1 OP



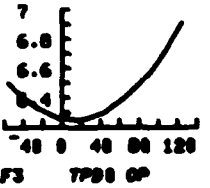
B0-P TPD1 OP



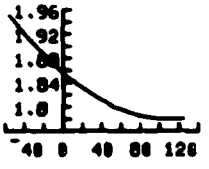
B1-G TPD0 OP



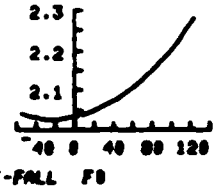
B0-A-B TPD1 OP



M-F3 TPD0 OP



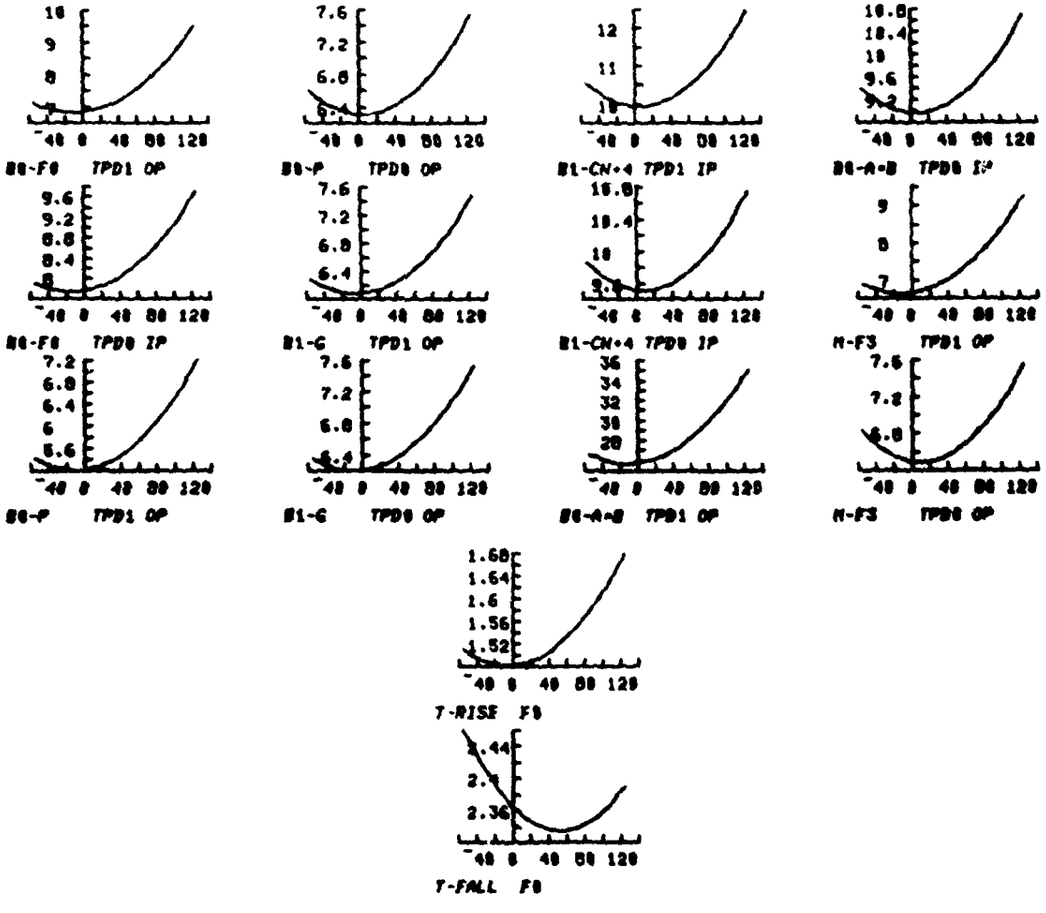
T-RISE F0



T-FALL F0

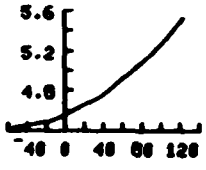
CIRCUIT TYPE FAIRCHILD FAST 161 DIFF MODE 50PF 10/31/88 8:42:24

DELAY PATH		LOAD 50 PF 5.5 VOLTS								
		MINIMUM			AVERAGE			MAXIMUM		
		-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
B0-F0	TPD1 OP	6.7	6.6	8.8	7.1	7.8	9.5	7.3	7.2	10.9
B0-F0	TPD0 IP	7.8	7.3	9.3	7.9	7.9	9.7	8.2	8.1	10.2
B0-P	TPD1 OP	5.4	5.1	6.7	5.4	5.3	7.2	5.5	5.5	7.6
B0-P	TPD0 OP	6.5	6.8	7.1	6.6	6.3	7.5	6.8	6.5	7.9
B1-G	TPD1 OP	6.2	5.8	7.1	6.3	6.2	7.5	6.3	6.3	7.9
B1-G	TPD0 OP	6.3	6.1	7.1	6.4	6.3	7.5	6.4	6.6	7.9
B1-CN+4	TPD1 IP	10.3	9.8	11.6	10.6	10.8	12.5	10.8	10.4	13.1
B1-CN+4	TPD0 IP	9.8	9.2	10.4	9.9	9.5	10.8	10.0	9.8	11.1
B0-A+B	TPD1 OP	26.4	26.1	32.9	26.7	26.4	35.1	27.8	26.6	36.3
B0-A+B	TPD0 IP	9.2	8.5	10.2	9.4	9.8	10.7	9.6	9.2	11.1
M-F3	TPD1 OP	6.8	6.5	8.6	6.9	6.8	9.3	7.8	7.1	9.6
M-F3	TPD0 OP	6.6	6.2	7.3	6.8	6.5	7.6	7.4	6.7	7.8
T-RISE	F0	1.5	1.4	1.5	1.5	1.5	1.7	1.6	1.5	1.8
T-FALL	F0	2.3	2.3	2.3	2.5	2.3	2.4	2.9	2.5	2.4

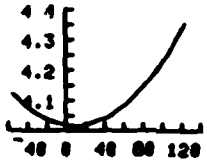


CIRCUIT TYPE TEXAS INSTR. AS882 50PF 10/23/88 13:19:42

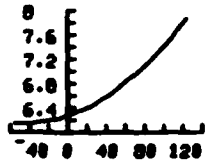
DELAY PATH	LOAD	50 PF		5.0 VOLTS					
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
Y3-CN+32 TPD1	3.8	4.2	5.2	4.4	4.7	5.5	4.6	4.9	5.7
Y3-CN+32 TPD0	5.5	5.8	6.3	5.6	5.4	5.6	5.7	5.6	7.7
X6-CN+32 TPD1	3.2	3.5	4.3	3.8	3.9	4.6	4.8	4.1	4.7
X6-CN+32 TPD0	4.1	3.9	4.3	4.1	4.8	4.4	4.2	4.1	4.5
X8-CN+8 TPD1	2.8	3.1	4.1	2.9	3.2	4.1	3.8	3.3	4.2
X8-CN+8 TPD0	4.6	4.5	4.7	4.7	4.6	4.8	4.8	4.8	4.9
CN-CN+32 TPD1	5.3	5.8	7.5	6.2	6.5	7.9	6.5	6.7	8.3
CN-CN+32 TPD0	7.2	7.5	8.5	7.4	7.8	8.8	7.5	7.9	9.7
CN-CN+24 TPD1	5.7	5.6	7.5	5.9	6.1	7.6	6.2	6.3	7.9
CN-CN+24 TPD0	6.3	6.6	7.9	6.6	6.9	8.2	6.7	8.9	9.3
CN-CN+8 TPD1	4.3	4.5	5.8	4.4	4.6	6.8	4.5	4.7	6.3
CN-CN+8 TPD0	6.1	6.2	7.5	6.4	6.5	8.3	6.8	6.7	8.6
T-RISE CN+32	1.2	1.1	1.2	1.4	1.3	1.3	1.4	1.4	1.4
T-FALL CN+32	2.6	2.6	3.1	2.7	2.9	3.2	3.1	3.2	3.8



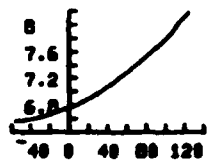
Y3-CN+32 TPD1



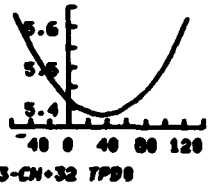
X6-CN+32 TPD0



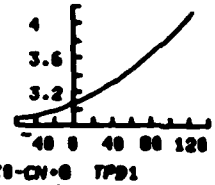
CN-CN+32 TPD1



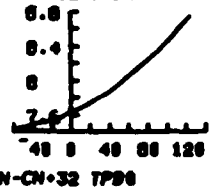
CN-CN+24 TPD0



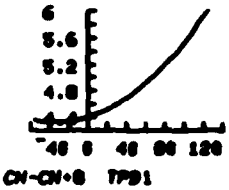
Y3-CN+32 TPD0



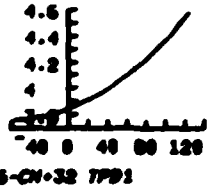
X8-CN+8 TPD1



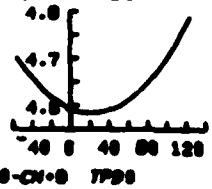
CN-CN+32 TPD0



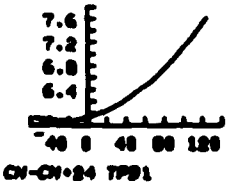
CN-CN+8 TPD1



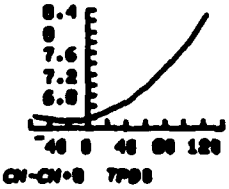
X6-CN+32 TPD1



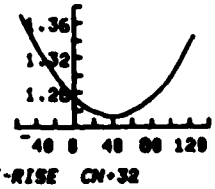
X8-CN+8 TPD0



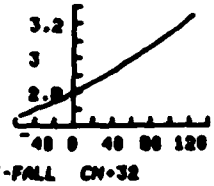
CN-CN+24 TPD1



CN-CN+8 TPD0



T-RISE CN+32

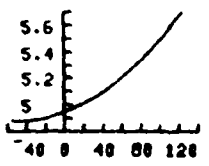


T-FALL CN+32

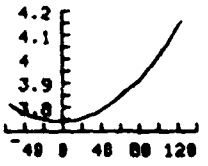
CIRCUIT TYPE TEXAS INSTR. AS882 50PF 10/23/80 13:17:50

LOAD 50 PF 4.5 VOLTS

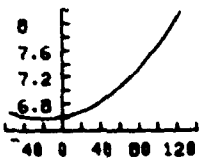
DELAY PATH	MINIMUM -55 C	MINIMUM 25 C	MINIMUM 125 C	AVERAGE -55 C	AVERAGE 25 C	AVERAGE 125 C	MAXIMUM -55 C	MAXIMUM 25 C	MAXIMUM 125 C
Y3-CN+32 TPD1	4.8	4.3	5.2	4.9	5.0	5.7	5.1	5.3	5.9
Y3-CN+32 TPD0	5.6	5.0	5.2	5.6	5.4	5.6	5.7	5.6	7.0
X6-CN+32 TPD1	3.4	3.7	4.4	4.2	4.3	4.0	4.5	4.4	4.9
X6-CN+32 TPD0	3.7	3.7	4.1	3.8	3.8	4.2	3.9	3.8	4.2
X0-CN+0 TPD1	3.0	3.2	4.1	3.1	3.3	4.2	3.2	3.3	4.3
X0-CN+0 TPD0	4.4	4.4	4.6	4.5	4.5	4.7	4.7	4.0	4.0
CN-CN+32 TPD1	5.0	6.0	7.6	6.7	6.7	0.2	7.0	7.0	0.7
CN-CN+32 TPD0	7.2	7.4	0.3	7.4	7.7	0.6	7.5	7.0	9.6
CN-CN+24 TPD1	6.2	5.9	7.5	6.4	6.3	7.0	6.6	6.6	0.1
CN-CN+24 TPD0	6.2	6.6	7.7	6.5	7.0	7.9	6.6	9.3	9.3
CN-CN+0 TPD1	4.6	4.5	5.9	4.7	4.6	6.0	4.0	4.0	6.4
CN-CN+0 TPD0	6.0	6.0	7.2	6.3	6.5	0.1	6.5	6.6	0.3
T-RISE CN+32	1.2	1.2	1.3	1.6	1.5	1.5	1.7	1.5	1.5
T-FALL CN+32	2.2	2.4	2.0	2.3	2.6	3.0	2.9	3.0	3.6



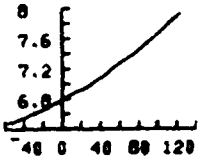
Y3-CN+32 TPD1



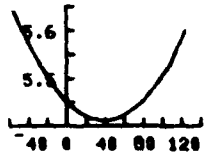
X6-CN+32 TPD0



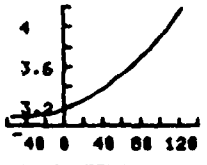
CN-CN+32 TPD1



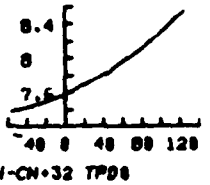
CN-CN+24 TPD0



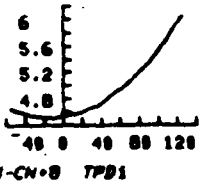
Y3-CN+32 TPD0



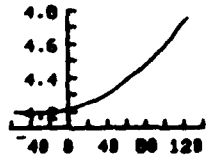
X0-CN+0 TPD1



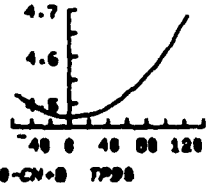
CN-CN+32 TPD0



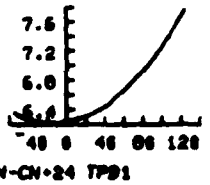
CN-CN+0 TPD1



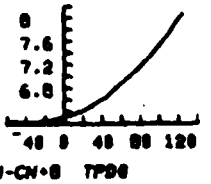
X6-CN+32 TPD1



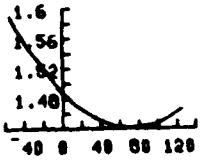
X0-CN+0 TPD0



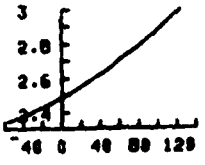
CN-CN+24 TPD1



CN-CN+0 TPD0



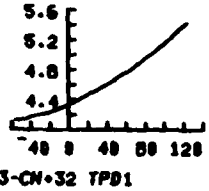
T-RISE CN+32



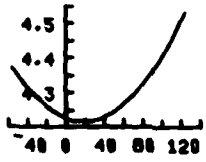
T-FALL CN+32

CIRCUIT TYPE TEXAS INSTR. AS882 50PF 10/23/88 13:21:35

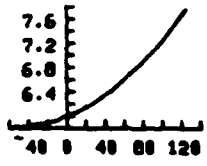
DELAY PATH	LOAD 50 PF 5.5 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
Y3-CN+32 TPD1	3.6	4.8	5.2	4.1	4.5	5.4	4.3	4.8	5.6
Y3-CN+32 TPD0	5.6	4.9	5.3	5.7	5.4	5.7	5.8	5.6	7.6
X6-CN+32 TPD1	3.1	3.4	4.3	3.5	3.7	4.5	3.7	3.8	4.6
X6-CN+32 TPD0	4.3	4.1	4.5	4.4	4.2	4.5	4.5	4.3	4.6
X0-CN+0 TPD1	2.8	3.1	4.0	2.8	3.2	4.1	2.9	3.2	4.2
X0-CN+0 TPD0	4.7	4.5	4.8	4.8	4.7	4.9	5.0	4.8	5.1
CN-CN+32 TPD1	5.1	5.6	7.5	5.8	6.2	7.8	6.2	6.5	8.3
CN-CN+32 TPD0	7.3	7.6	8.7	7.5	7.8	8.9	7.6	7.9	9.7
CN-CN+24 TPD1	5.4	5.3	7.3	5.6	5.9	7.6	5.8	6.1	7.8
CN-CN+24 TPD0	6.4	6.6	8.1	6.6	7.0	8.3	6.7	8.6	9.4
CN-CN+0 TPD1	4.1	4.5	5.8	4.2	4.6	6.0	4.4	4.7	6.4
CN-CN+0 TPD0	6.3	6.3	7.8	6.6	6.7	8.5	6.9	6.9	8.8
T-RISE CN+32	1.1	1.1	1.2	1.2	1.1	1.2	1.3	1.2	1.3
T-FALL CN+32	2.8	2.9	3.3	2.9	3.1	3.5	3.4	3.4	4.0



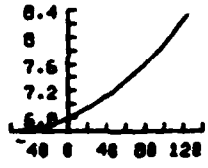
Y3-CN+32 TPD1



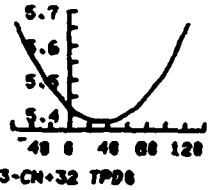
X6-CN+32 TPD0



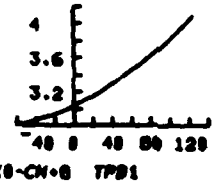
CN-CN+32 TPD1



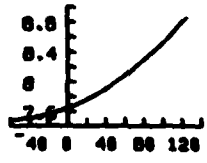
CN-CN+24 TPD0



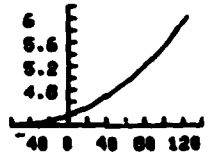
Y3-CN+32 TPD0



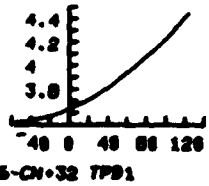
X0-CN+0 TPD1



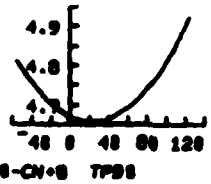
CN-CN+32 TPD0



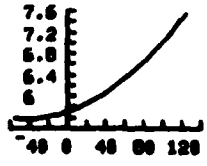
CN-CN+0 TPD1



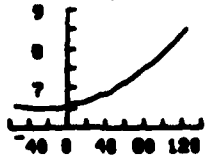
X6-CN+32 TPD1



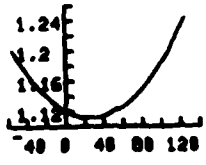
X0-CN+0 TPD0



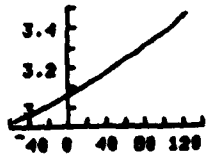
CN-CN+24 TPD1



CN-CN+0 TPD0



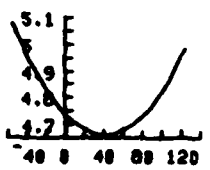
T-RISE CN+32



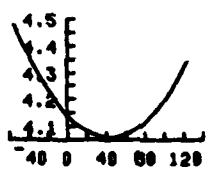
T-FALL CN+32

CIRCUIT TYPE FAIRCHILD 74F11 DC 8836 10/07/88 8:56:54

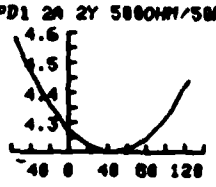
DELAY PATH	LOAD 0 PF 5.0 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
TPD1 2A 2Y 500OHM/50PF	4.0	4.4	4.5	5.1	4.7	5.0	5.3	5.0	5.2
TPD0 2A 2Y 500OHM/50PF	4.2	4.0	4.3	4.6	4.2	4.4	4.9	4.4	4.6
TPD1 3A 3Y 1-30OHM COAX	4.2	3.7	4.0	4.5	4.0	4.5	4.6	4.2	4.9
TPD0 3A 3Y 1-30OHM COAX	4.0	3.8	4.2	4.5	4.1	4.3	4.8	4.2	4.4
TRISE AT 3Y .5U-1.5U	1.1	1.1	1.2	1.3	1.2	1.5	1.4	1.3	1.7
TFALL AT 3Y 2.6U-1.6U	.0	.6	.6	.0	.6	.6	1.0	.0	.6



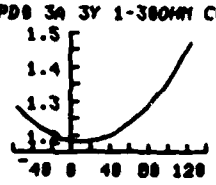
TPD1 2A 2Y 500OHM/50PF



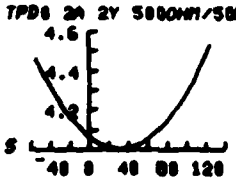
TPD0 3A 3Y 1-30OHM COAX



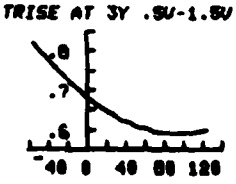
TPD0 2A 2Y 500OHM/50PF



TRISE AT 3Y .5U-1.5U



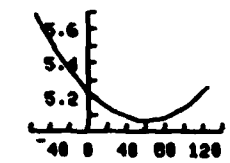
TPD1 3A 3Y 1-30OHM COAX



TFALL AT 3Y 2.6U-1.6U

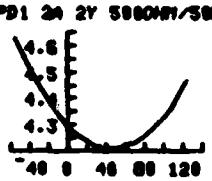
CIRCUIT TYPE FAIRCHILD 74F11 DC 8036 10/07/88 8:55:58

DELAY PATH	LOAD 0 PF 4.5 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
TPD1 2A 2Y 500OHM/50PF	5.4	4.8	4.8	5.7	5.1	5.3	6.0	5.4	5.5
TPD0 2A 2Y 500OHM/50PF	4.2	3.9	4.3	4.6	4.2	4.5	5.0	4.4	4.6
TPD1 3A 3Y 1-380HM COAX	4.6	4.1	4.2	5.0	4.4	4.7	5.1	4.6	5.0
TPD0 3A 3Y 1-380HM COAX	4.2	4.0	4.2	4.6	4.2	4.4	4.0	4.4	4.4
TRISE AT 3Y .5V-1.5V	1.4	1.2	1.4	1.7	1.4	1.6	1.0	1.6	1.0
TFALL AT 3Y 2.6V-1.6V	1.0	.0	.6	3.0	.9	.0	4.0	1.0	.0

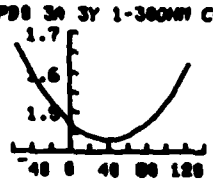


TPD1 2A 2Y 500OHM/50PF

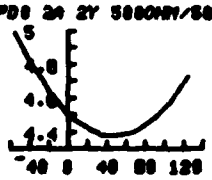
TPD0 3A 3Y 1-380HM COAX



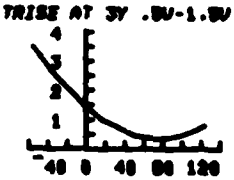
TPD0 2A 2Y 500OHM/50PF



TRISE AT 3Y .5V-1.5V



TPD1 3A 3Y 1-380HM COAX

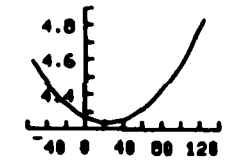


TFALL AT 3Y 2.6V-1.6V

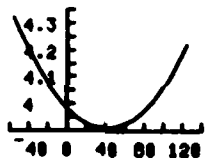
CIRCUIT TYPE FAIRCHILD 74F11 DC 8836 10/07/80 8:57:58

DELAY [illegible] LOAD 8 PF 5.5 VOLTS

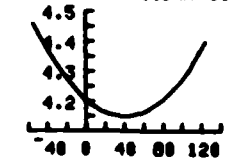
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
TPD1 2A 2Y 500OHM/50PF	4.4	3.9	4.3	4.6	4.2	4.8	4.8	4.5	5.1
TPD0 2A 2Y 500OHM/50PF	4.1	3.9	4.2	4.5	4.2	4.4	4.8	4.3	4.6
TPD1 3A 3Y 1-38OHM COAX	3.8	3.4	3.8	4.1	3.7	4.4	4.2	3.8	4.8
TPD0 3A 3Y 1-38OHM COAX	4.0	3.6	4.2	4.3	3.9	4.2	4.6	4.2	4.4
TRISE AT 3Y .5V-1.5V	1.0	.9	1.1	1.1	1.0	1.4	1.1	1.0	1.6
TFALL AT 3Y 2.6V-1.6V	.6	.4	.4	.7	.5	.5	.8	.6	.6



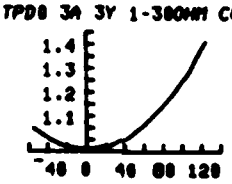
TPD1 2A 2Y 500OHM/50PF



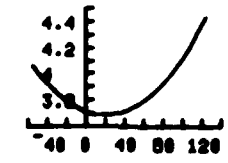
TPD0 3A 3Y 1-38OHM COAX



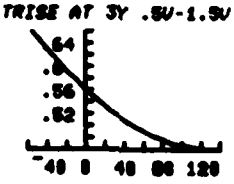
TPD0 2A 2Y 500OHM/50PF



TRISE AT 3Y .5V-1.5V



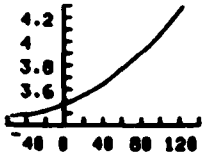
TPD1 3A 3Y 1-38OHM COAX



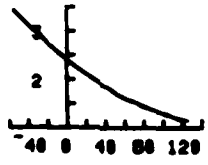
TFALL AT 3Y 2.6V-1.6V

CIRCUIT TYPE FAIRCHILD 54F20 [illegible]14/88 [illegible]:15

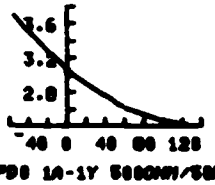
DELAY PATH	LOAD	0	PF	5.0	VOLTS					
	MINIMUM			AVERAGE			MAXIMUM			
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C	
TPD1 1A-1Y 500OHM/50PF	3.3	3.4	4.1	3.4	3.6	4.3	3.5	3.8	4.5	
TPD0 1A-1Y 500OHM/50PF	3.3	2.6	2.3	3.7	2.9	2.4	4.1	3.5	2.5	
TPD1 2D-2Y 30 OHM COAX	3.8	3.1	4.0	3.1	3.2	4.2	3.1	3.4	4.5	
TPD0 2D-2Y 30 OHM COAX	2.9	1.7	1.0	3.4	2.8	1.2	3.9	2.7	1.3	
TRISE 1Y 10-/--1.5V	1.8	1.7	1.6	1.8	1.7	1.7	1.9	1.8	1.7	
TFALL 1Y 90-/--1.5V	1.9	1.8	1.7	2.1	1.9	1.8	2.4	2.2	1.8	



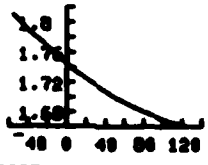
TPD1 1A-1Y 500OHM/50PF



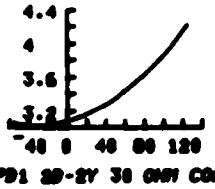
TPD0 2D-2Y 30 OHM COAX



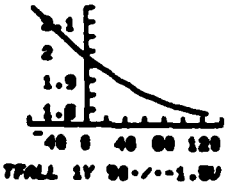
TPD0 1A-1Y 500OHM/50PF



TRISE 1Y 10-/--1.5V



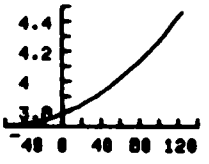
TPD1 2D-2Y 30 OHM COAX



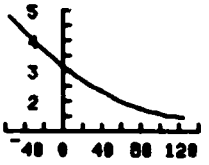
TFALL 1Y 90-/--1.5V

CIRCUIT TYPE FAIRCHILD S4F20 8/14/86 15:37:20

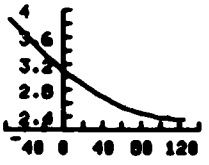
DELAY PATH	LOAD 0 PF 4.5 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
TPD1 1A-1Y 500OHM/50PF	3.6	3.7	4.3	3.7	3.9	4.5	3.8	4.1	4.7
TPD0 1A-1Y 500OHM/50PF	3.4	2.6	2.2	3.9	2.8	2.4	4.3	3.5	2.4
TPD1 2D-2Y 30 OHM COAX	3.7	3.6	4.4	3.8	3.7	4.6	3.9	4.0	4.8
TPD0 2D-2Y 30 OHM COAX	4.0	2.2	1.3	4.0	2.6	1.4	5.0	3.4	1.6
TRISE 1Y 10%/--1.5V	2.1	1.9	1.8	2.2	2.0	1.9	2.2	2.1	2.0
TFALL 1Y 90%/--1.5V	1.8	1.7	1.7	2.0	1.8	1.7	2.4	2.0	1.8



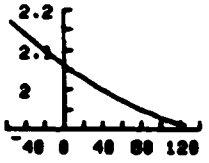
TPD1 1A-1Y 500OHM/50PF



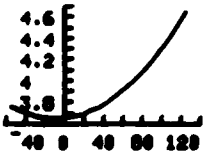
TPD0 2D-2Y 30 OHM COAX



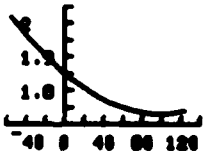
TPD0 1A-1Y 500OHM/50PF



TRISE 1Y 10%/--1.5V



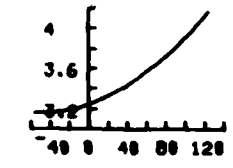
TPD1 2D-2Y 30 OHM COAX



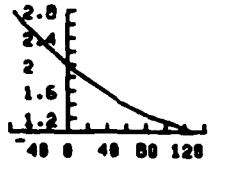
TFALL 1Y 90%/--1.5V

CIRCUIT TYPE FAIRCHILD 54F20 8/14/88 15:39:09

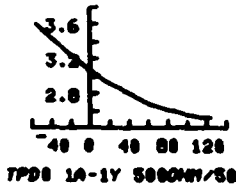
DELAY PATH	LOAD 0 PF 5.5 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
TPD1 1A-1Y 500OHM/50PF	3.1	3.3	4.0	3.2	3.4	4.2	3.2	3.6	4.4
TPD0 1A-1Y 500OHM/50PF	3.2	2.7	2.5	3.6	2.9	2.5	4.0	3.5	2.6
TPD1 2D-2Y 30 OHM COAX	2.6	2.7	3.7	2.7	2.9	3.9	2.7	3.1	4.2
TPD0 2D-2Y 30 OHM COAX	2.3	1.4	1.0	2.0	1.7	1.0	3.1	2.3	1.1
TRISE 1Y 10-/--1.5V	1.5	1.4	1.4	1.5	1.5	1.5	1.6	1.5	1.5
TFALL 1Y 90-/--1.5V	2.1	1.0	1.0	2.3	2.0	1.9	2.4	2.3	1.9



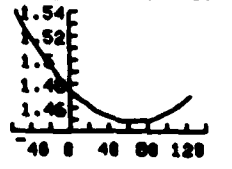
TPD1 1A-1Y 500OHM/50PF



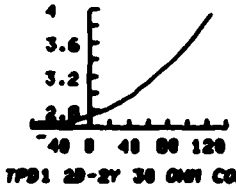
TPD0 2D-2Y 30 OHM COAX



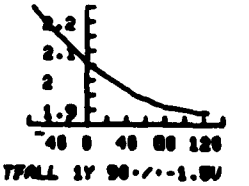
TPD0 1A-1Y 500OHM/50PF



TRISE 1Y 10-/--1.5V



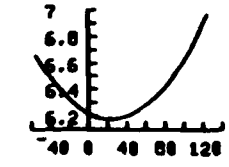
TPD1 2D-2Y 30 OHM COAX



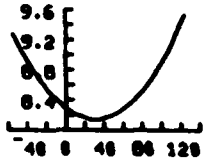
TFALL 1Y 90-/--1.5V

CIRCUIT TYPE FAIRCHILD FAST 374 6/09/80 10:20:00

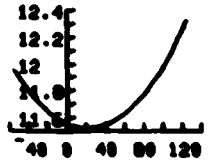
DELAY PATH	5.0 VOLTS MINIMUM -55 C	25 C	125 C	AVERAGE -55 C	25 C	125 C	MAXIMUM -55 C	25 C	125 C
CLK-10 50PF TPD1	6.1	5.6	6.3	6.6	6.2	7.0	7.0	6.6	7.4
CLK-10 50PF TPD0	6.5	5.8	7.1	7.1	6.5	8.0	7.5	7.0	8.0
CLK-20 150PF TPD1	7.9	7.4	8.4	9.0	8.4	9.1	9.4	8.9	9.6
CLK-20 150PF TPD0	8.7	7.6	8.7	9.3	8.1	9.5	9.7	8.7	9.9
CLK-30 250PF TPD1	10.0	10.0	10.4	11.3	10.5	11.1	11.7	11.1	11.6
CLK-30 250PF TPD0	10.4	9.2	10.3	11.0	10.0	11.1	12.0	10.3	11.5
CLK-60 30K TPD1	11.5	10.9	11.6	12.0	11.5	12.3	12.3	12.0	12.0
CLK-60 30K TPD0	11.9	11.3	12.4	12.5	12.0	13.2	13.0	12.5	13.6
THZ	4.3	3.9	3.1	4.5	4.1	4.0	4.9	4.3	4.1
TLZ	6.7	6.3	7.0	7.7	7.1	9.5	12.3	10.4	12.1
TZH	4.4	4.2	4.0	4.6	4.5	5.1	4.0	4.6	5.5
TZL	4.9	4.9	5.7	5.4	5.3	6.2	5.6	5.5	6.5
TRISE 10 50PF	1.2	1.1	1.2	1.3	1.2	1.3	1.3	1.2	1.3
TFALL 10 50PF	1.3	1.4	1.5	1.5	1.5	1.6	1.6	1.6	1.8



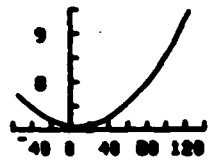
CLK-10 50PF TPD1



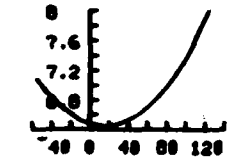
CLK-20 150PF TPD0



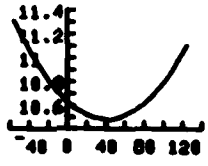
CLK-60 30K TPD1



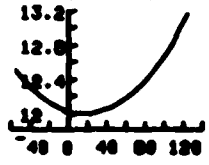
TLZ



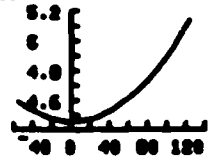
CLK-10 50PF TPD0



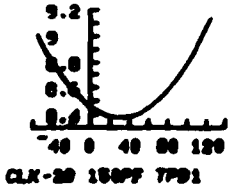
CLK-30 250PF TPD1



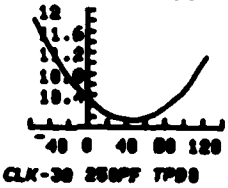
CLK-60 30K TPD0



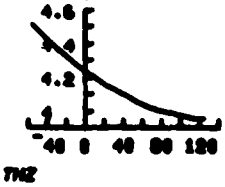
TZH



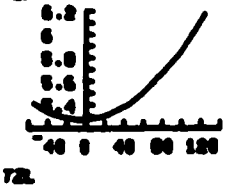
CLK-20 150PF TPD1



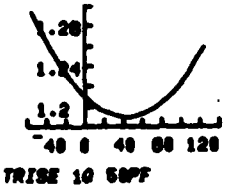
CLK-30 250PF TPD0



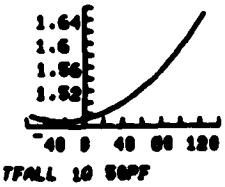
THZ



TZL



TRISE 10 50PF

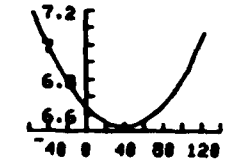


TFALL 10 50PF

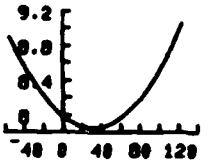
CIRCUIT TYPE FAIRCHILD FAST 374 6/09/88 10:18:07

4.5 VOLTS

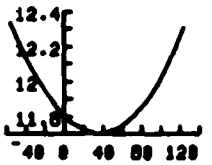
DELAY PATH	MINIMUM -55 C	MINIMUM 25 C	MINIMUM 125 C	AVERAGE -55 C	AVERAGE 25 C	AVERAGE 125 C	MAXIMUM -55 C	MAXIMUM 25 C	MAXIMUM 125 C
CLK-10 50PF TPD1	6.6	6.9	6.4	7.2	6.8	7.1	7.6	7.8	7.6
CLK-10 50PF TPD0	6.4	6.7	6.7	7.0	6.3	7.6	7.4	6.8	8.8
CLK-20 150PF TPD1	9.1	8.3	8.9	10.3	9.3	9.6	10.7	9.8	10.1
CLK-20 150PF TPD0	8.4	7.3	8.2	8.9	7.9	9.1	9.2	8.4	9.6
CLK-30 250PF TPD1	12.7	11.4	11.4	13.2	11.9	12.1	13.7	12.3	12.6
CLK-30 250PF TPD0	9.9	8.8	9.8	11.4	9.7	10.6	11.9	10.8	10.9
CLK-60 30X TPD1	11.8	11.1	11.6	12.3	11.7	12.3	12.7	12.2	12.8
CLK-60 30X TPD0	12.1	11.3	12.8	12.6	12.8	12.8	13.8	12.5	13.3
TMZ	5.1	4.7	3.6	5.2	4.8	4.6	5.6	5.8	4.8
TLZ	7.2	6.5	7.5	8.1	7.4	9.2	8.9	11.4	12.4
TZH	4.9	4.6	5.1	5.1	4.9	5.4	5.3	5.1	5.7
TZL	4.7	4.8	5.6	5.2	5.2	6.0	5.5	5.4	6.3
TRISE 10 50PF	1.5	1.4	1.3	1.6	1.4	1.4	1.6	1.5	1.6
TFALL 10 50PF	.9	1.1	1.4	1.0	1.2	1.4	1.1	1.2	1.5



CLK-10 50PF TPD1

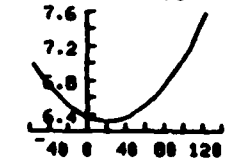


CLK-20 150PF TPD0

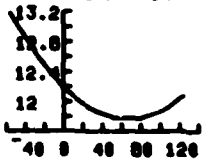


CLK-60 30X TPD1

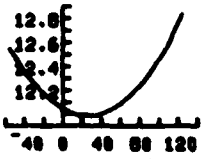
TLZ



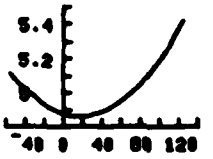
CLK-10 50PF TPD0



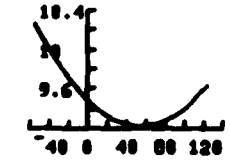
CLK-30 250PF TPD1



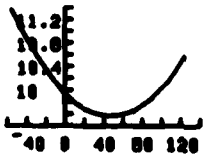
CLK-60 30X TPD0



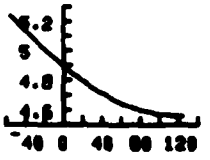
TZH



CLK-20 150PF TPD1

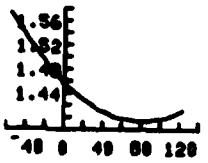


CLK-30 250PF TPD0

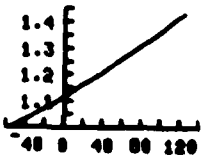


TMZ

TZL



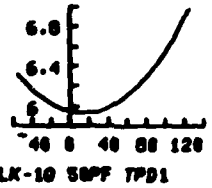
TRISE 10 50PF



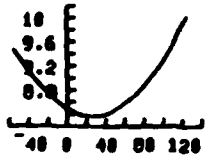
TFALL 10 50PF

CIRCUIT TYPE FAIRCHILD FAST 374 6/09/88 10:21:54

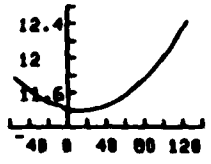
DELAY PATH	5.5 VOLTS MINIMUM -55 C	25 C	125 C	AVERAGE -55 C	25 C	125 C	MAXIMUM -55 C	25 C	125 C
CLK-10 50PF TPD1	5.8	5.3	6.3	6.3	5.9	7.8	6.7	6.5	7.4
CLK-10 50PF TPD0	6.7	6.8	7.5	7.2	6.6	8.4	7.6	7.1	8.9
CLK-20 150PF TPD1	7.2	7.8	8.2	8.3	7.9	8.9	8.8	8.4	9.4
CLK-20 150PF TPD0	8.9	7.8	9.2	9.5	8.4	10.8	9.8	8.9	10.5
CLK-30 250PF TPD1	9.7	9.0	9.9	10.2	9.6	10.6	10.7	10.2	11.1
CLK-30 250PF TPD0	10.6	9.4	10.7	12.4	10.4	11.7	13.3	10.7	12.2
CLK-60 30X TPD1	11.2	10.8	11.6	11.8	11.4	12.4	12.2	12.8	12.9
CLK-60 30X TPD0	12.1	11.4	12.7	12.6	12.1	13.5	13.1	12.6	13.9
THZ	4.8	3.8	3.1	4.1	3.8	3.7	4.3	4.8	3.8
TLZ	6.4	6.1	8.8	7.4	6.9	9.9	10.7	9.8	11.9
TZH	3.9	3.9	4.6	4.2	4.2	5.8	4.4	4.3	5.3
TZL	5.8	5.9	5.8	5.5	5.4	6.3	5.7	5.6	6.6
TRISE 10 50PF	1.8	1.8	1.1	1.1	1.8	1.2	1.1	1.1	1.2
TFALL 10 50PF	1.6	1.6	1.7	1.8	1.7	1.8	1.9	1.8	1.9



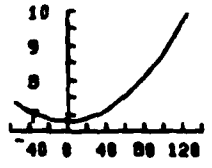
CLK-10 50PF TPD1



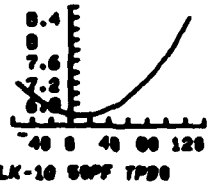
CLK-20 150PF TPD0



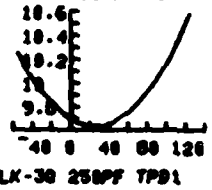
CLK-60 30X TPD1



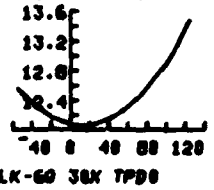
TLZ



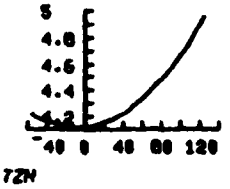
CLK-10 50PF TPD0



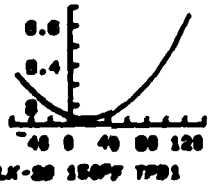
CLK-30 250PF TPD1



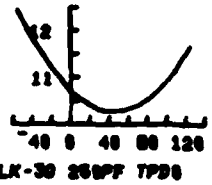
CLK-60 30X TPD0



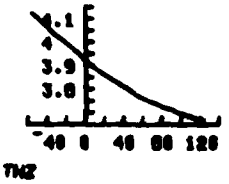
TZH



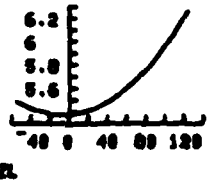
CLK-20 150PF TPD1



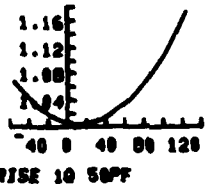
CLK-30 250PF TPD0



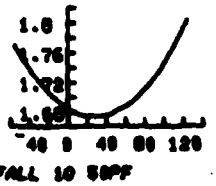
THZ



TZL



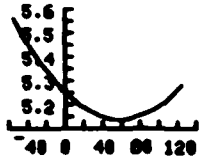
TRISE 10 50PF



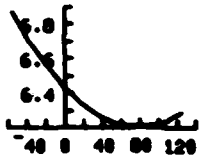
TFALL 10 50PF

CIRCUIT TYPE FAIRCHILD 54F175 DC0050 1/13/81 15:37:21

DELAY PATH	LOAD 50 PF 5.0 VOLTS	MINIMUM			AVERAGE			MAXIMUM		
		-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
TPD1 CX-20	5080HW50PF	5.5	5.0	5.2	5.6	5.2	5.3	5.7	5.2	5.3
TPD0 CX-20	5080HW50PF	6.5	5.9	6.2	6.5	6.1	6.3	6.8	6.2	6.4
TPD1 CX-20BAR	5080HW50PF	5.3	4.9	5.1	5.4	5.0	5.2	5.5	5.1	5.3
TPD0 CX-20BAR	5080HW50PF	6.8	6.1	6.2	6.9	6.3	6.3	7.0	6.5	6.4
TPD1 CLR-20BAR	5080HW50PF	6.4	6.1	6.6	6.5	6.2	6.7	6.6	6.3	6.8
TPD0 CLR-20	5080HW50PF	7.7	6.9	7.4	7.9	7.2	7.7	7.9	7.4	7.8
TPD1 CX-40	380HB00NTLN	4.8	4.3	4.6	5.0	4.6	4.7	5.1	4.7	4.8
TPD0 CX-40	380HB00NTLN	6.8	5.8	6.0	7.0	6.1	6.2	7.2	6.4	6.4
TPD1 CX-40BAR	380HB00NTLN	4.9	4.4	4.6	4.9	4.5	4.7	5.1	4.7	4.8
TPD0 CX-40BAR	380HB00NTLN	6.4	5.6	5.8	6.5	5.8	5.9	6.6	6.2	6.0
TPD1 CLR-40BAR	380HB00NTLN	6.0	5.6	6.2	6.1	5.8	6.4	6.1	6.0	6.5
TPD0 CLR-40	380HB00NTLN	8.0	7.0	7.6	8.1	7.2	7.7	8.2	7.4	7.8
TRISE AT 40 1V-2V		1.0	.9	.9	1.1	.9	1.0	1.1	1.0	1.0
TFALL AT 40 2V-1V		2.0	1.2	.8	2.2	1.4	.9	2.4	1.8	1.0

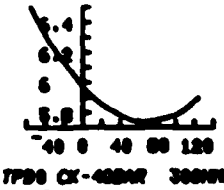


TPD1 CX-20 5080HW50PF

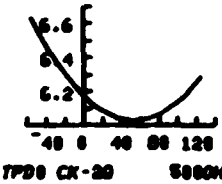


TPD0 CX-20BAR 5080HW50PF

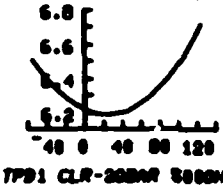
TPD1 CX-40 380HB00NTLN



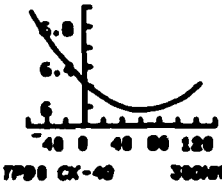
TPD0 CX-40BAR 380HB00NTLN



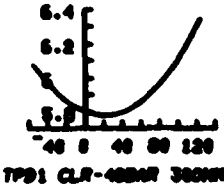
TPD0 CX-20 5080HW50PF



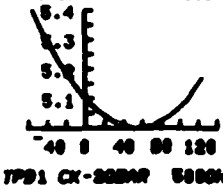
TPD1 CLR-20BAR 5080HW50PF



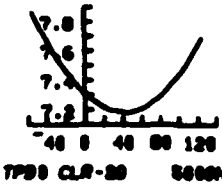
TPD0 CX-40 380HB00NTLN



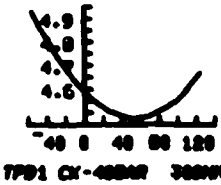
TPD1 CLR-40BAR 380HB00NTLN



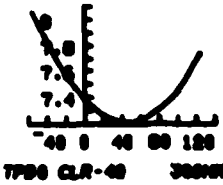
TPD1 CX-20BAR 5080HW50PF



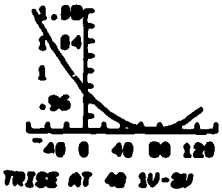
TPD0 CLR-20 5080HW50PF



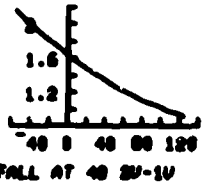
TPD1 CX-40BAR 380HB00NTLN



TPD0 CLR-40 380HB00NTLN



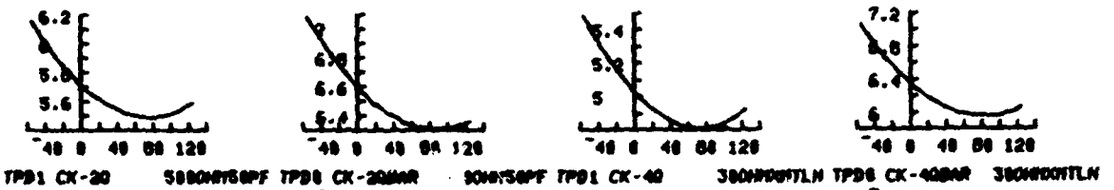
TRISE AT 40 1V-2V

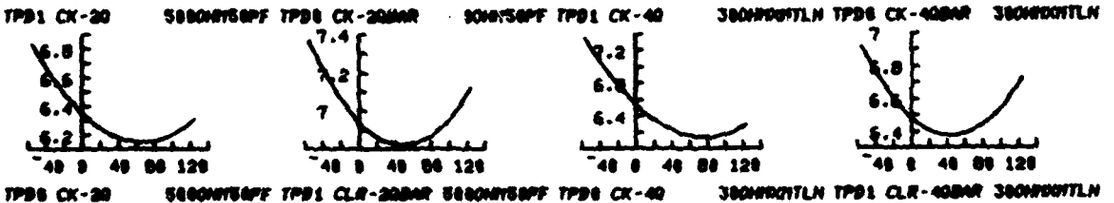


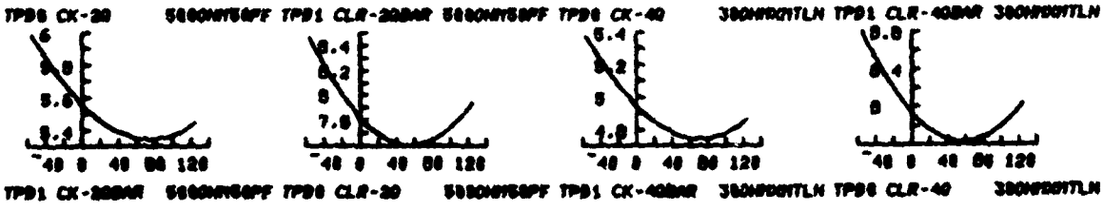
TFALL AT 40 2V-1V

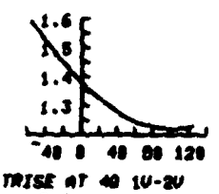
CIRCUIT TYPE FAIRCHILD 54F175 DC8868 1/13/81 15:34:58

DELAY PATH	LOAD	50 PF 4.5 VOLTS								
		MINIMUM			AVERAGE			MAXIMUM		
		-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
TPD1 CK-Q	5880H75QPF	6.0	5.4	5.5	6.2	5.6	5.6	6.3	5.7	5.6
TPD0 CK-Q	5880H75QPF	6.0	6.0	6.2	6.8	6.2	6.3	7.0	6.3	6.4
TPD1 CK-QBAR	5880H75QPF	5.9	5.3	5.4	6.0	5.4	5.4	6.1	5.5	5.5
TPD0 CK-QBAR	5880H75QPF	7.0	6.2	6.3	7.1	6.5	6.4	7.3	6.6	6.4
TPD1 CLR-QBAR	5880H75QPF	7.3	6.6	6.9	7.4	6.8	7.1	7.4	7.0	7.2
TPD0 CLR-Q	5880H75QPF	8.3	7.2	7.8	8.6	7.7	7.9	8.6	7.9	8.1
TPD1 CK-Q	380H00NTLN	5.3	4.7	4.9	5.5	4.9	4.9	5.6	5.0	5.0
TPD0 CK-Q	380H00NTLN	7.2	6.0	6.2	7.3	6.3	6.3	7.6	6.4	6.4
TPD1 CK-QBAR	380H00NTLN	5.3	4.7	4.8	5.4	4.8	4.9	5.5	4.9	4.9
TPD0 CK-QBAR	380H00NTLN	6.8	6.0	5.8	7.1	6.1	6.1	7.2	6.4	6.2
TPD1 CLR-QBAR	380H00NTLN	6.8	6.1	6.6	6.9	6.4	6.7	7.0	6.6	6.9
TPD0 CLR-Q	380H00NTLN	8.6	7.4	7.8	8.8	7.7	8.0	9.0	8.0	8.2
TRISE AT 4Q 1V-2V		1.5	1.2	1.2	1.6	1.3	1.2	1.6	1.4	1.3
TFALL AT 4Q 2V-1V		2.2	1.6	1.8	2.4	1.8	1.1	2.6	2.2	1.2



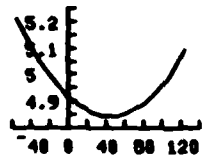




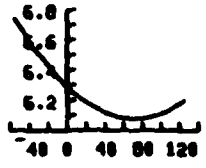


CIRCUIT TYPE FAIRCHILD 54F176 DC0060 1/13/91 15:39:05

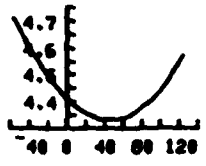
DELAY PATH	LOAD	50 PF 5.5 VOLTS MINIMUM -55 C	25 C	125 C	AVERAGE -55 C	25 C	125 C	MAXIMUM -55 C	25 C	125 C
TPD1 CK-20	5080H975DPF	5.1	4.7	5.0	5.2	4.9	5.1	5.4	4.9	5.1
TPD0 CK-20	5080H975DPF	6.3	5.8	6.1	6.4	6.0	6.3	6.6	6.1	6.4
TPD1 CK-20BAR	5080H975DPF	5.0	4.6	4.9	5.1	4.7	5.0	5.1	4.8	5.0
TPD0 CK-20BAR	5080H975DPF	6.7	5.9	6.1	6.7	6.2	6.2	6.9	6.3	6.3
TPD1 CLR-20BAR	5080H975DPF	5.8	5.6	6.3	5.9	5.7	6.5	6.0	5.8	6.6
TPD0 CLR-20	5080H975DPF	7.2	6.5	7.4	7.4	6.9	7.6	7.5	7.1	7.7
TPD1 CK-40	380H900TLN	4.6	4.2	4.5	4.7	4.3	4.6	4.8	4.4	4.7
TPD0 CK-40	380H900TLN	6.6	5.8	6.0	6.7	5.9	6.2	6.8	6.0	6.4
TPD1 CK-40BAR	380H900TLN	4.6	4.2	4.5	4.6	4.3	4.6	4.7	4.4	4.7
TPD0 CK-40BAR	380H900TLN	6.0	5.4	5.6	6.1	5.6	5.8	6.2	5.8	5.8
TPD1 CLR-40BAR	380H900TLN	5.5	5.2	6.0	5.6	5.3	6.2	5.7	5.5	6.3
TPD0 CLR-40	380H900TLN	7.4	6.6	7.6	7.5	6.9	7.6	7.8	7.0	7.6
TRISE AT 40 1V-2V		.8	.7	.7	.8	.8	.8	.9	.8	.9
TFALL AT 40 2V-1V		1.6	1.8	.6	1.8	1.1	.7	2.8	1.4	.8



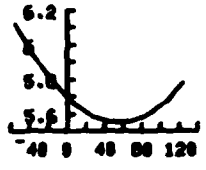
TPD1 CK-20 5080H975DPF



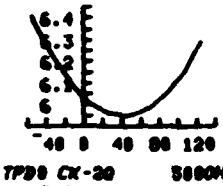
TPD0 CK-20BAR 5080H975DPF



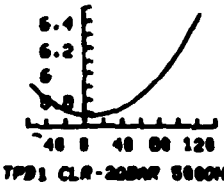
TPD1 CK-40 380H900TLN



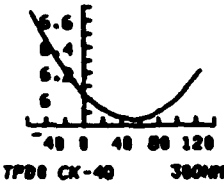
TPD0 CK-40BAR 380H900TLN



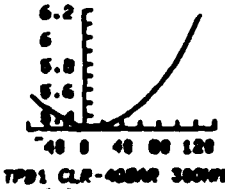
TPD0 CK-20 5080H975DPF



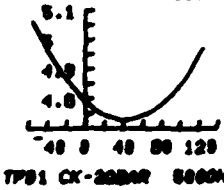
TPD1 CLR-20BAR 5080H975DPF



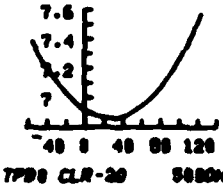
TPD0 CK-40 380H900TLN



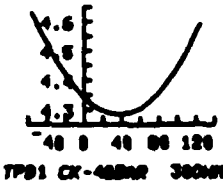
TPD1 CLR-40BAR 380H900TLN



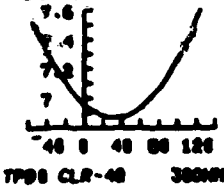
TPD1 CK-20BAR 5080H975DPF



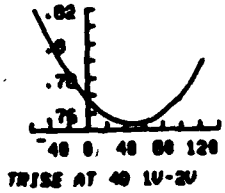
TPD0 CLR-20 5080H975DPF



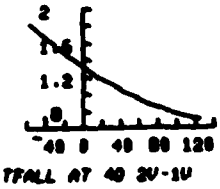
TPD1 CK-40BAR 380H900TLN



TPD0 CLR-40 380H900TLN



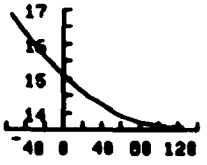
TRISE AT 40 1V-2V



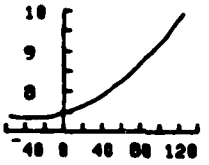
TFALL AT 40 2V-1V

CIRCUIT TYPE T.I. ALS11 DC8020 10/24/80 13:25:21

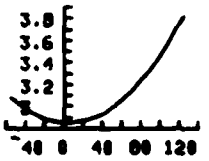
DELAY PATH	LOAD 50 PF 5.0 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
TPD1 1C-1Y 500OHM/50PF	15.4	13.4	13.0	16.9	14.5	13.6	18.0	15.6	14.4
TPD0 1C-1Y 500OHM/50PF	7.3	8.0	9.9	7.7	8.1	10.2	7.9	8.4	11.0
TPD1 2C-2Y 500OHM/50PF	10.4	9.4	10.2	11.1	9.7	10.7	11.0	10.2	12.2
TPD0 2C-2Y 500OHM/50PF	7.3	7.5	9.6	7.4	7.7	9.9	7.5	8.0	10.6
TPD1 3A-3Y 500OHM/50PF	11.0	10.4	11.2	12.7	10.9	11.0	13.6	11.6	13.2
TPD0 3A-3Y 500OHM/50PF	7.3	7.7	9.0	7.6	8.0	10.1	8.4	8.4	10.7
TRISE AT 1Y .3V-1.3V	2.0	2.6	3.4	3.1	2.9	3.0	3.2	3.2	5.0
TFALL AT 1Y 2.3V-1.3V	3.2	2.2	2.2	3.4	2.4	2.2	3.6	2.6	2.4
TRISE AT 2Y .3V-1.3V	2.0	3.0	3.0	3.0	3.2	4.2	3.2	3.6	5.4
TFALL AT 2Y 2.3V-1.3V	2.0	2.0	2.0	3.2	2.2	2.2	3.2	2.4	2.4
TRISE AT 3Y .3V-1.3V	3.0	2.0	3.0	3.1	3.1	4.2	3.6	3.4	5.6
TFALL AT 3Y 2.3V-1.3V	3.2	2.2	2.0	3.4	2.3	2.1	3.6	2.4	2.2



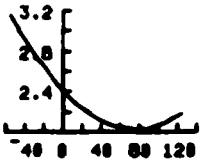
TPD1 1C-1Y 500OHM/50PF



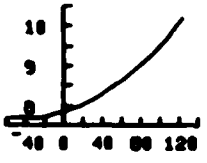
TPD0 2C-2Y 500OHM/50PF



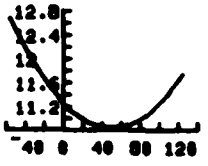
TRISE AT 1Y .3V-1.3V



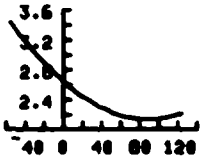
TFALL AT 2Y 2.3V-1.3V



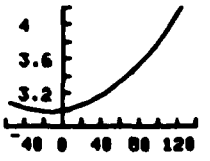
TPD0 1C-1Y 500OHM/50PF



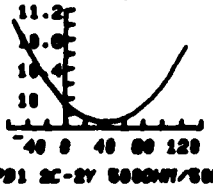
TPD1 3A-3Y 500OHM/50PF



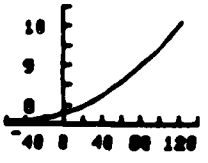
TFALL AT 1Y 2.3V-1.3V



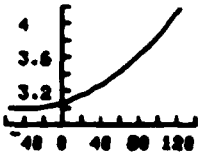
TRISE AT 3Y .3V-1.3V



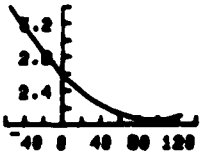
TPD1 2C-2Y 500OHM/50PF



TPD0 3A-3Y 500OHM/50PF



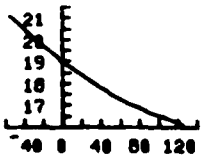
TRISE AT 2Y .3V-1.3V



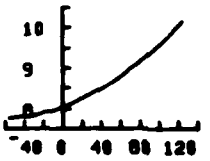
TFALL AT 3Y 2.3V-1.3V

CIRCUIT TYPE T.J. ALS11 DC0820 10/24/80 13:23:43

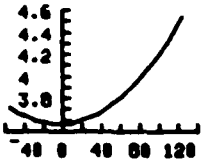
DELAY PATH	LOAD 50 PF 4.5 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
TPD1 1C-1Y 500OHM/50PF	19.4	16.8	15.8	21.1	18.2	16.1	22.4	19.6	17.0
TPD0 1C-1Y 500OHM/50PF	7.7	8.5	10.1	8.8	8.7	10.4	8.1	9.0	11.1
TPD1 2C-2Y 500OHM/50PF	12.6	11.2	11.4	13.7	11.5	11.8	14.8	12.8	13.0
TPD0 2C-2Y 500OHM/50PF	7.6	8.0	9.9	7.8	8.3	10.2	8.0	8.4	10.6
TPD1 3A-3Y 500OHM/50PF	15.0	12.6	12.8	16.1	13.4	13.3	17.2	14.4	14.4
TPD0 3A-3Y 500OHM/50PF	7.9	8.4	10.1	8.1	8.6	10.4	8.7	8.9	10.9
TRISE AT 1Y .3V-1.3V	3.6	3.4	4.2	3.7	3.6	4.5	4.0	4.0	5.0
TFALL AT 1Y 2.3V-1.3V	4.0	3.0	2.0	5.0	4.0	2.9	5.2	4.2	3.2
TRISE AT 2Y .3V-1.3V	3.0	3.2	4.2	3.4	3.4	4.5	3.6	3.0	5.6
TFALL AT 2Y 2.3V-1.3V	4.4	3.6	2.0	4.7	3.7	2.0	4.0	3.0	3.0
TRISE AT 3Y .3V-1.3V	3.6	3.4	4.2	3.0	3.6	4.7	4.2	3.0	6.0
TFALL AT 3Y 2.3V-1.3V	4.0	3.0	2.0	5.2	4.0	2.0	5.6	4.2	3.2



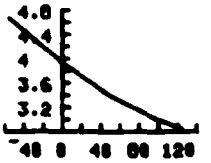
TPD1 1C-1Y 500OHM/50PF



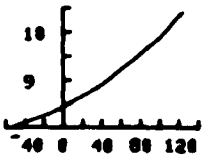
TPD0 2C-2Y 500OHM/50PF



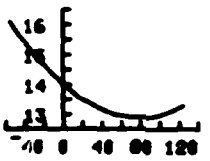
TRISE AT 1Y .3V-1.3V



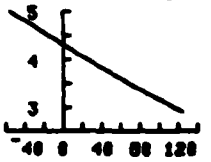
TFALL AT 2Y 2.3V-1.3V



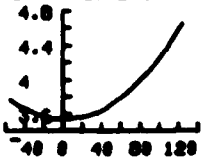
TPD0 1C-1Y 500OHM/50PF



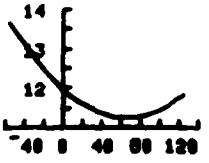
TPD1 3A-3Y 500OHM/50PF



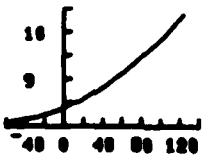
TFALL AT 1Y 2.3V-1.3V



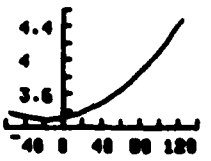
TRISE AT 3Y .3V-1.3V



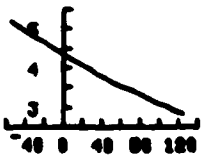
TPD1 2C-2Y 500OHM/50PF



TPD0 3A-3Y 500OHM/50PF



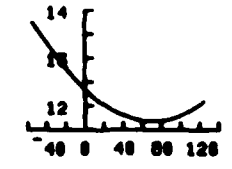
TRISE AT 2Y .3V-1.3V



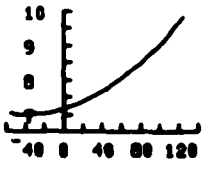
TFALL AT 3Y 2.3V-1.3V

CIRCUIT TYPE T.I. ALS11 DC0828 10/24/88 13:27:01

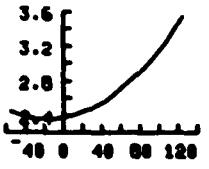
DELAY PATH	LOAD 50 PF 5.5 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
TPD1 1C-1Y 500OHM/50PF	12.4	11.2	11.6	13.0	12.0	12.1	14.6	12.0	13.2
TPD0 1C-1Y 500OHM/50PF	7.2	7.7	9.9	7.3	7.0	10.2	7.7	8.3	11.0
TPD1 2C-2Y 500OHM/50PF	9.0	8.0	9.2	9.3	8.3	9.0	10.0	8.0	11.4
TPD0 2C-2Y 500OHM/50PF	7.0	7.0	9.4	7.0	7.4	9.0	7.2	7.7	10.4
TPD1 3A-3Y 500OHM/50PF	10.0	9.0	10.2	10.5	9.4	10.6	11.0	9.0	12.2
TPD0 3A-3Y 500OHM/50PF	6.0	7.5	9.6	7.1	7.7	10.1	7.0	7.9	11.0
TRISE AT 1Y .3V-1.3V	2.2	2.2	3.2	2.4	2.5	3.5	2.6	2.0	4.0
TFALL AT 1Y 2.3V-1.3V	2.4	1.0	1.0	2.6	1.0	1.0	2.0	1.0	2.0
TRISE AT 2Y .3V-1.3V	2.6	2.6	3.6	2.0	2.0	3.9	3.0	3.2	5.0
TFALL AT 2Y 2.3V-1.3V	2.0	1.6	1.6	2.4	1.7	1.0	2.4	1.0	2.0
TRISE AT 3Y .3V-1.3V	2.6	2.6	3.6	2.7	2.0	3.9	3.0	3.2	5.2
TFALL AT 3Y 2.3V-1.3V	2.4	1.0	1.6	2.4	1.0	1.0	2.4	1.0	2.0



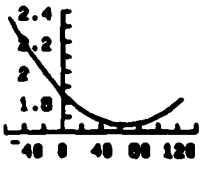
TPD1 1C-1Y 500OHM/50PF



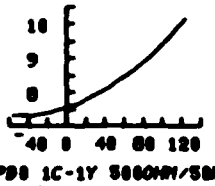
TPD0 2C-2Y 500OHM/50PF



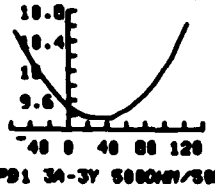
TRISE AT 1Y .3V-1.3V



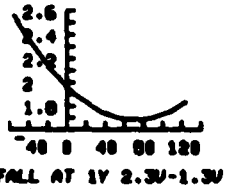
TFALL AT 2Y 2.3V-1.3V



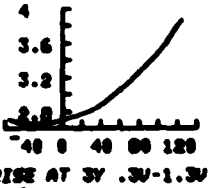
TPD0 1C-1Y 500OHM/50PF



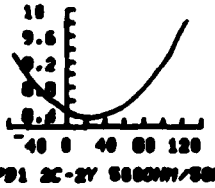
TPD1 3A-3Y 500OHM/50PF



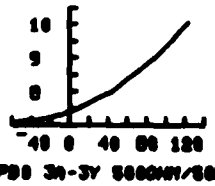
TFALL AT 1Y 2.3V-1.3V



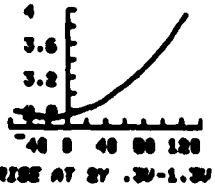
TRISE AT 3Y .3V-1.3V



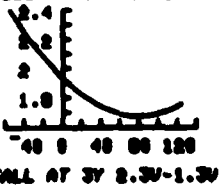
TPD1 2C-2Y 500OHM/50PF



TPD0 3A-3Y 500OHM/50PF



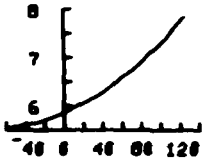
TRISE AT 2Y .3V-1.3V



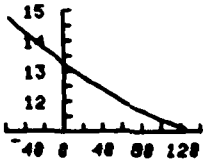
TFALL AT 3Y 2.3V-1.3V

CIRCUIT TYPE T.I. 54ALS20 (THRESHOLD=1.3V)

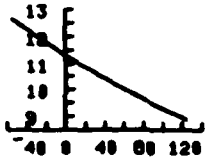
DELAY PATH	LOAD 0 PF 5.0 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
TPD1 1A-1Y 500OHM/50PF	5.4	5.9	7.1	5.6	6.1	7.9	5.8	6.4	8.4
TPD0 1A-1Y 500OHM/50PF	11.7	8.7	7.9	12.7	10.7	8.9	13.6	11.9	10.8
TPD1 2D-2Y 30 OHM COAX	4.3	4.9	6.0	4.6	5.1	6.8	5.0	5.5	7.1
TPD0 2D-2Y 30 OHM COAX	13.0	11.1	9.5	14.7	12.7	11.1	16.0	14.0	12.5
TRISE 1.0V-2.0V 1Y (50PF)	2.4	2.4	2.8	2.6	2.6	3.2	2.8	2.8	3.6
TFALL 2.0V-1.0V 1Y (50PF)	2.6	2.1	2.0	2.7	2.3	2.1	2.9	2.5	2.3



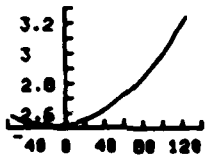
TPD1 1A-1Y 500OHM/50PF



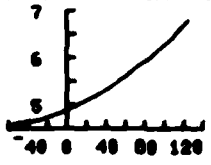
TPD0 2D-2Y 30 OHM COAX



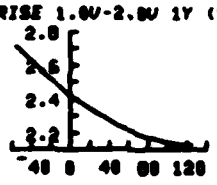
TPD0 1A-1Y 500OHM/50PF



TRISE 1.0V-2.0V 1Y (50PF)



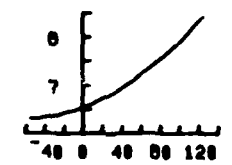
TPD1 2D-2Y 30 OHM COAX



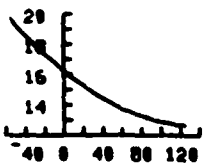
TFALL 2.0V-1.0V 1Y (50PF)

CIRCUIT TYPE T.I. 54ALS20 (THRESHOLD=1.3V) 8/22/88 9:37:38

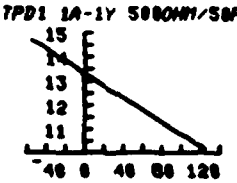
DELAY PATH	LOAD 0 PF 4.5 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
TPD1 1A-1Y 500OHM/50PF	6.1	6.5	7.6	6.3	6.8	8.4	6.6	7.1	9.8
TPD0 1A-1Y 500OHM/50PF	13.5	10.1	8.9	14.7	12.7	10.2	15.8	14.8	11.6
TPD1 2D-2Y 30 OHM COAX	5.2	5.5	6.7	5.4	5.9	7.6	5.8	6.4	8.2
TPD0 2D-2Y 30 OHM COAX	17.9	13.3	10.6	19.7	15.0	12.7	20.6	16.6	14.5
TRISE 1.0V-2.0V 1Y (50PF)	3.2	3.0	3.5	3.5	3.2	4.0	3.9	3.6	4.5
TFALL 2.0V-1.0V 1Y (50PF)	3.9	3.1	2.5	4.1	3.5	2.8	4.3	3.8	3.3



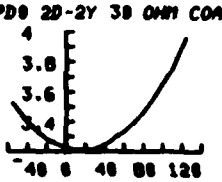
TPD1 1A-1Y 500OHM/50PF



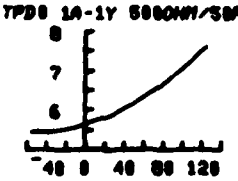
TPD0 2D-2Y 30 OHM COAX



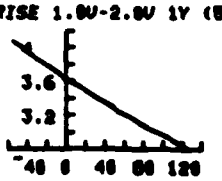
TPD0 1A-1Y 500OHM/50PF



TRISE 1.0V-2.0V 1Y (50PF)



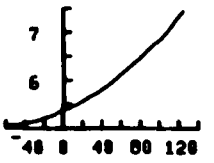
TPD1 2D-2Y 30 OHM COAX



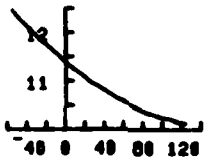
TFALL 2.0V-1.0V 1Y (50PF)

CIRCUIT TYPE T.I. 54ALS20 (THRESHOLD=1.3V) 8/22/88 9:39:19

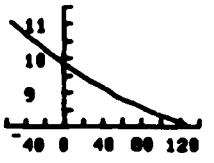
DELAY PATH	LOAD 0 PF 5.5 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
TPD1 1A-1Y 500OHM/50PF	4.9	5.5	6.6	5.1	5.6	7.4	5.3	5.9	7.9
TPD0 1A-1Y 500OHM/50PF	10.2	7.8	7.3	11.1	9.4	8.1	11.9	10.4	8.8
TPD1 2D-2Y 30 OHM COAX	3.8	4.4	5.3	4.0	4.6	6.2	4.2	5.8	6.5
TPD0 2D-2Y 30 OHM COAX	11.0	9.6	8.9	12.5	11.0	10.1	13.6	12.2	11.1
TRISE 1.0V-2.0V 1Y (50PF)	2.0	2.1	2.4	2.1	2.2	2.0	2.3	2.4	3.2
TFALL 2.0V-1.0V 1Y (50PF)	1.9	1.7	1.6	1.9	1.0	1.7	2.1	1.9	1.9



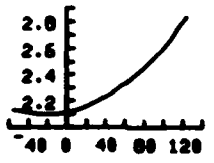
TPD1 1A-1Y 500OHM/50PF



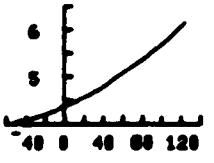
TPD0 2D-2Y 30 OHM COAX



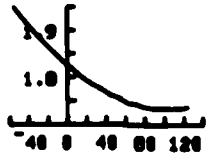
TPD0 1A-1Y 500OHM/50PF



TRISE 1.0V-2.0V 1Y (50PF)



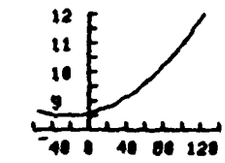
TPD1 2D-2Y 30 OHM COAX



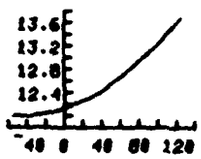
TFALL 2.0V-1.0V 1Y (50PF)

CIRCUIT TYPE TEXAS INSTR. ALS74 (FINAL) 8/25/88 15:39:17

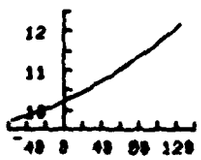
DELAY PATH	LOAD 50 PF 5.0 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
CLK-1Q TPD1	8.4	8.5	10.8	8.6	8.9	12.8	8.8	9.1	14.4
CLK-1Q TPD0	11.3	11.7	12.9	11.8	12.3	13.9	12.1	12.7	14.4
CLK-1QBAR TPD1	8.9	9.8	10.8	9.1	9.3	12.1	9.4	9.7	13.1
CLK-1QBAR TPD0	11.6	11.5	12.6	12.8	12.3	13.7	12.4	12.8	14.4
PSET-1Q TPD1	7.8	7.6	9.8	7.2	7.8	9.5	7.4	8.3	10.2
PSET-1QBAR TPD0	10.1	10.4	11.9	10.4	11.1	12.4	10.7	11.4	12.9
CLR-1Q TPD0	9.3	10.2	11.6	9.7	10.5	12.2	10.8	10.8	12.6
CLR-1QBAR TPD1	7.8	7.6	9.3	7.2	8.8	9.9	7.6	8.4	10.8
CLK-2Q TPD1 30X	7.8	7.2	9.4	7.3	7.6	10.4	7.5	7.9	12.6
CLK-2Q TPD0 30X	11.8	11.8	13.8	11.8	12.9	15.6	12.4	13.6	17.2
CLK-2QBAR TPD1 30X	7.8	7.9	10.1	8.1	8.4	11.4	8.4	9.1	13.1
CLK-2QBAR TPD0 30X	11.8	11.4	12.8	11.7	12.5	14.8	12.2	13.4	16.2
T-RISE 20 30X	2.8	3.8	4.3	3.1	3.4	5.8	3.4	3.6	7.2
T-FALL 20 30X	3.6	3.4	4.4	4.2	4.8	4.8	4.6	4.4	5.2



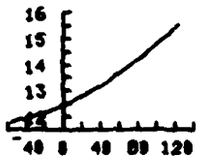
CLK-1Q TPD1



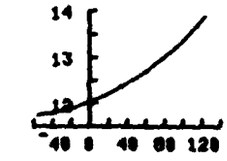
CLK-1QBAR TPD0



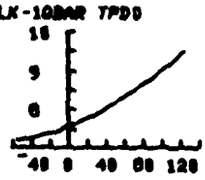
CLR-1Q TPD0



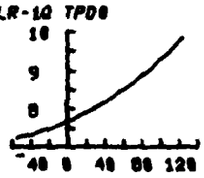
CLK-2Q TPD0 30X



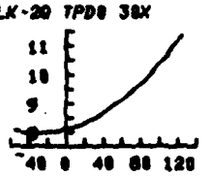
CLK-1Q TPD0



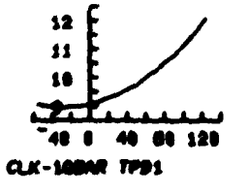
PSET-1Q TPD1



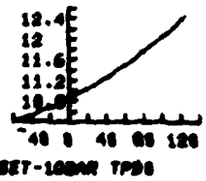
CLR-1QBAR TPD1



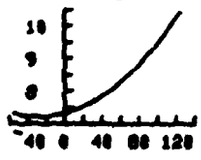
CLK-2QBAR TPD1 30X



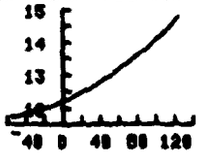
CLK-1QBAR TPD1



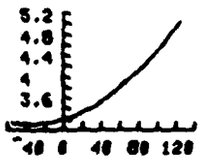
PSET-1QBAR TPD0



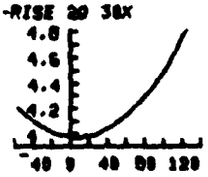
CLK-2Q TPD1 30X



CLK-2QBAR TPD0 30X



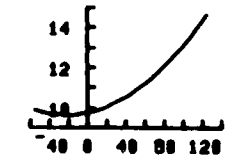
T-RISE 20 30X



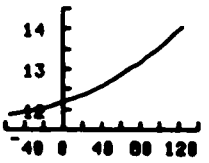
T-FALL 20 30X

CIRCUIT TYPE TEXAS INSTR. ALS74 (FINAL) 8/25/88 15:37:27

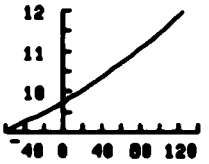
DELAY PATH	LOAD 50 PF 4.5 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
CLK-1Q TPD1	9.6	9.5	12.2	9.9	10.2	14.6	10.1	10.7	17.0
CLK-1Q TPD0	11.4	12.0	13.3	11.8	12.4	14.2	12.1	13.0	14.8
CLK-1QBAR TPD1	9.9	10.0	12.6	10.3	10.6	14.4	10.6	11.2	16.2
CLK-1QBAR TPD0	11.6	11.6	13.1	11.9	12.4	14.0	12.3	12.9	14.8
PSET-1Q TPD1	7.8	8.3	9.8	8.0	8.6	10.4	8.3	9.0	11.1
PSET-1QBAR TPD0	9.3	9.7	11.0	9.5	10.5	12.2	9.7	10.9	12.4
CLR-1Q TPD0	8.8	9.7	11.5	9.1	10.1	12.0	9.3	10.4	12.3
CLR-1QBAR TPD1	7.9	8.4	10.1	8.2	8.8	10.7	8.6	9.3	11.7
CLK-2Q TPD1 30X	8.3	8.1	10.8	8.6	9.0	12.4	9.1	9.7	14.0
CLK-2Q TPD0 30X	11.2	12.4	13.8	10.5	13.4	16.3	27.4	14.2	18.2
CLK-2QBAR TPD1 30X	9.1	9.1	11.0	9.5	9.8	14.1	10.1	10.8	16.6
CLK-2QBAR TPD0 30X	11.2	12.2	13.8	10.4	13.1	15.5	27.6	13.8	16.6
T-RISE 20 30X	3.6	3.7	5.3	4.8	4.3	6.4	4.4	4.7	7.6
T-FALL 20 30X	4.6	4.4	5.4	12.1	5.1	6.1	21.2	5.8	6.6



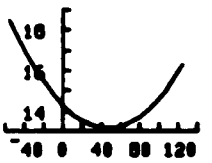
CLK-1Q TPD1



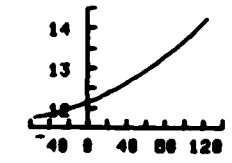
CLK-1QBAR TPD0



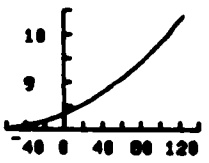
CLR-1Q TPD0



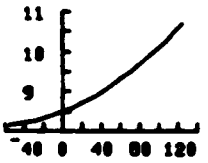
CLK-2Q TPD0 30X



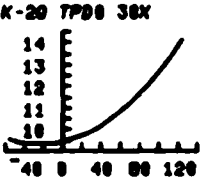
CLK-1Q TPD0



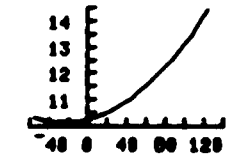
PSET-1Q TPD1



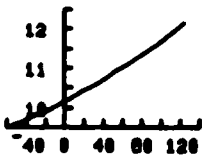
CLR-1QBAR TPD1



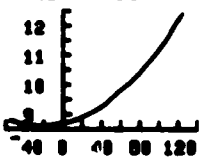
CLK-2QBAR TPD1 30X



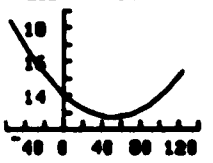
CLK-1QBAR TPD1



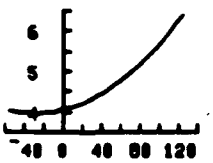
PSET-1QBAR TPD0



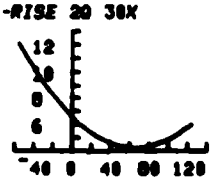
CLK-2Q TPD1 30X



CLK-2QBAR TPD0 30X



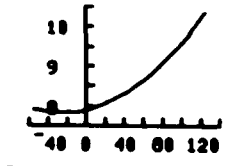
T-RISE 20 30X



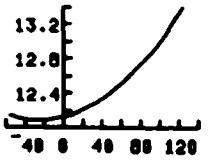
T-FALL 20 30X

CIRCUIT TYPE TEXAS INSTR. ALS74 (FINAL) 8/25/88 15:41:11

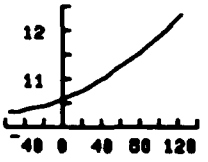
DELAY PATH	LOAD 50 PF 5.5 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
CLK-1Q TPD1	7.8	7.9	9.6	7.9	8.1	10.3	8.8	8.4	11.3
CLK-1Q TPD0	11.3	11.2	12.5	11.9	12.1	13.6	12.4	12.7	14.1
CLK-1QBAR TPD1	8.0	8.3	9.7	8.3	8.6	10.7	8.5	8.9	12.1
CLK-1QBAR TPD0	11.3	11.0	12.2	12.1	12.2	13.4	12.7	12.9	14.2
PSET-1Q TPD1	6.4	7.0	8.2	6.6	7.2	8.9	6.7	7.6	9.6
PSET-1QBAR TPD0	10.1	10.4	11.7	11.0	11.4	12.6	11.5	11.9	13.3
CLR-1Q TPD0	9.0	10.3	11.5	10.3	10.8	12.4	10.7	11.1	12.9
CLR-1QBAR TPD1	6.5	7.0	8.5	6.6	7.4	9.3	7.0	7.0	10.3
CLK-2Q TPD1 30X	6.2	6.5	8.3	6.5	6.8	9.0	6.6	7.1	9.9
CLK-2Q TPD0 30X	11.0	11.2	12.0	11.0	12.0	14.0	12.4	13.6	16.4
CLK-2QBAR TPD1 30X	6.9	7.2	8.9	7.1	7.5	10.0	7.4	7.9	11.4
CLK-2QBAR TPD0 30X	10.6	11.0	12.0	11.5	12.3	14.1	12.2	13.0	15.4
T-RISE 20 30X	2.3	2.5	3.7	2.6	2.0	4.0	2.0	3.0	4.4
T-FALL 20 30X	3.2	3.2	3.6	3.6	3.5	3.9	3.0	3.6	4.2



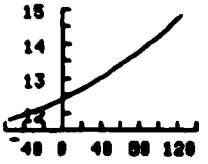
CLK-1Q TPD1



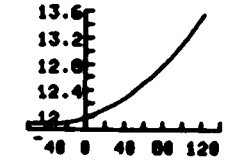
CLK-1QBAR TPD0



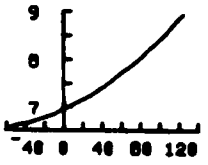
CLR-1Q TPD0



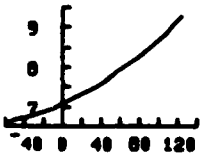
CLK-2Q TPD0 30X



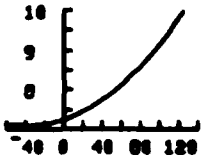
CLK-1Q TPD0



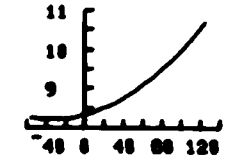
PSET-1Q TPD1



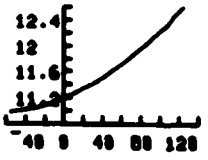
CLR-1QBAR TPD1



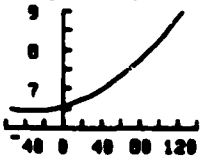
CLK-2QBAR TPD1 30X



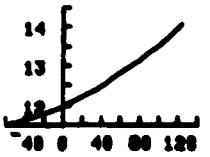
CLK-1QBAR TPD1



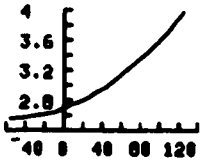
PSET-1QBAR TPD0



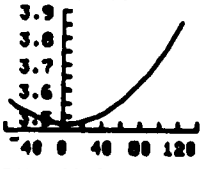
CLK-2Q TPD1 30X



CLK-2QBAR TPD0 30X



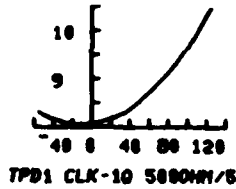
T-RISE 20 30X



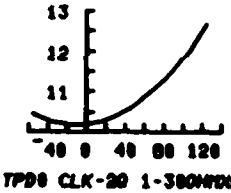
T-FALL 20 30X

CIRCUIT TYPE T.I. ALS574 DC8845 11/17/88 15:48:08

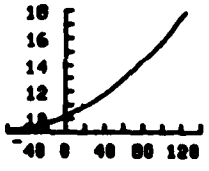
DELAY PATH	LOAD 50 PF 5.0 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
TPD1 CLK-1Q 500OHM/50PF	8.1	7.8	9.8	8.3	8.2	10.5	8.6	8.6	11.7
TPD0 CLK-1Q 500OHM/50PF	10.3	10.4	11.6	10.4	10.5	11.8	10.6	10.7	12.0
TPD1 CLK-2Q 1-380OHM/50PF	7.4	7.1	9.4	7.6	7.5	9.8	7.8	7.8	10.7
TPD0 CLK-2Q 1-380OHM/50PF	10.8	10.8	12.8	10.4	10.3	12.7	12.2	10.8	13.6
THZ OUTPUT CONTROL-3Q	5.8	5.4	5.4	5.9	5.5	5.5	6.0	5.6	5.8
TLZ OUTPUT CONTROL-3Q	7.0	7.2	12.4	7.1	7.5	13.2	7.2	7.8	14.4
TZH OUTPUT CONTROL-3Q	8.9	10.2	17.1	9.2	11.1	17.0	9.3	12.3	18.9
TZL OUTPUT CONTROL-3Q	10.9	11.4	14.2	11.1	11.6	14.5	11.4	12.0	14.9
TRISE AT 1Q 500OHM/50PF	1.9	1.9	3.1	2.0	2.1	3.6	2.1	2.2	4.7
TFALL AT 1Q 500OHM/50PF	2.0	2.0	2.4	2.0	2.0	2.6	2.1	2.1	2.7
TRISE AT 2Q 1-380OHM/50PF	1.8	1.8	3.0	1.8	1.9	3.5	1.9	2.0	4.6
TFALL AT 2Q 1-380OHM/50PF	1.8	1.8	2.4	1.8	1.9	2.7	2.0	2.0	3.0



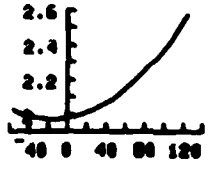
TPD1 CLK-1Q 500OHM/50PF



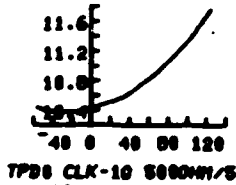
TPD0 CLK-2Q 1-380OHM/50PF



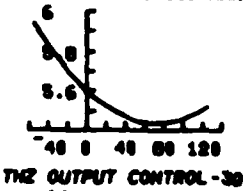
TZH OUTPUT CONTROL-3Q



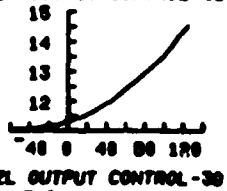
TFALL AT 1Q 500OHM/50PF



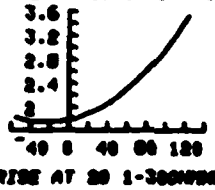
TPD0 CLK-1Q 500OHM/50PF



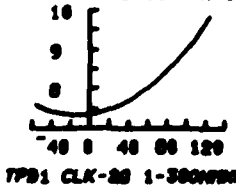
THZ OUTPUT CONTROL-3Q



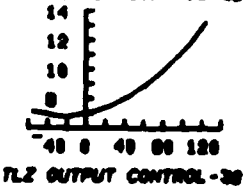
TZL OUTPUT CONTROL-3Q



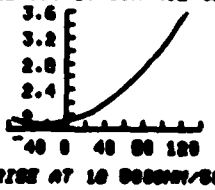
TRISE AT 2Q 1-380OHM/50PF



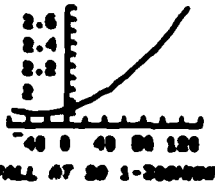
TPD1 CLK-2Q 1-380OHM/50PF



TLZ OUTPUT CONTROL-3Q



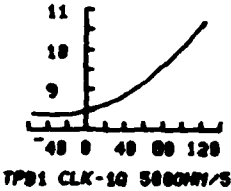
TRISE AT 1Q 500OHM/50PF



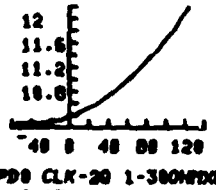
TFALL AT 2Q 1-380OHM/50PF

CIRCUIT TYPE T.I. ALS574 DC8045 11/17/88 15:38:27

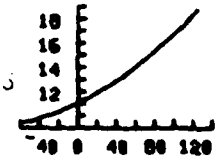
DELAY PATH	LOAD 50 PF 4.5 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
TPD1 CLK-1Q 500OHM/50PF	8.3	8.3	10.1	8.4	8.7	10.7	8.6	9.1	11.7
TPD0 CLK-1Q 500OHM/50PF	10.3	10.5	11.4	10.5	10.7	11.6	10.6	10.9	11.9
TPD1 CLK-2Q 1-380OHM/50TTLN	7.5	7.6	9.7	7.7	8.0	10.2	7.9	8.4	10.9
TPD0 CLK-2Q 1-380OHM/50TTLN	10.0	10.2	12.0	10.3	10.6	12.2	11.0	10.8	12.0
THZ OUTPUT CONTROL-3Q	6.0	6.0	5.0	6.1	6.1	6.1	6.2	6.2	6.2
TLZ OUTPUT CONTROL-3Q	7.0	7.2	11.6	7.1	7.5	12.1	7.2	7.6	12.0
TZH OUTPUT CONTROL-3Q	9.1	11.0	16.1	9.5	12.2	18.0	9.7	12.7	19.4
TZL OUTPUT CONTROL-3Q	11.1	12.0	15.5	11.3	13.1	15.7	11.0	13.4	16.1
TRISE AT 1Q 500OHM/50PF	1.9	2.2	3.5	2.0	2.4	4.0	2.1	2.5	5.1
TFALL AT 1Q 500OHM/50PF	2.1	2.4	2.9	2.1	2.5	3.0	2.2	2.6	3.1
TRISE AT 2Q 1-380OHM/50TTLN	1.0	2.1	3.5	1.9	2.3	4.1	2.0	2.4	5.1
TFALL AT 2Q 1-380OHM/50TTLN	1.0	2.2	2.0	1.9	2.4	3.1	2.0	2.6	3.2



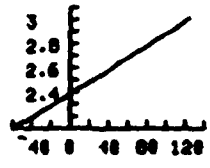
TPD1 CLK-1Q 500OHM/50PF



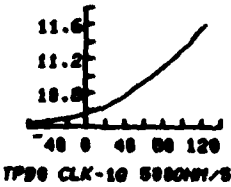
TPD0 CLK-2Q 1-380OHM/50TTLN



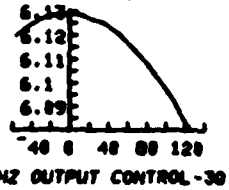
TZH OUTPUT CONTROL-3Q



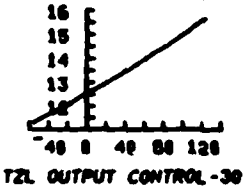
TFALL AT 1Q 500OHM/50PF



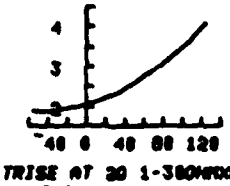
TPD0 CLK-1Q 500OHM/50PF



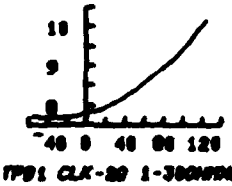
THZ OUTPUT CONTROL-3Q



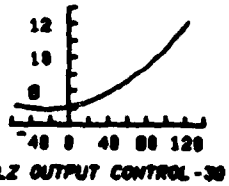
TZL OUTPUT CONTROL-3Q



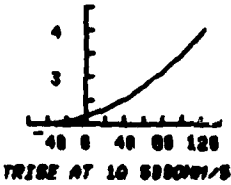
TRISE AT 2Q 1-380OHM/50TTLN



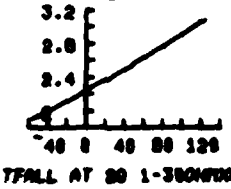
TPD1 CLK-2Q 1-380OHM/50TTLN



TLZ OUTPUT CONTROL-3Q



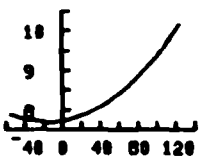
TRISE AT 1Q 500OHM/50PF



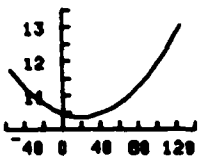
TFALL AT 2Q 1-380OHM/50TTLN

CIRCUIT TYPE T.I. ALS574 BC8045 11/17/88 15:41:55

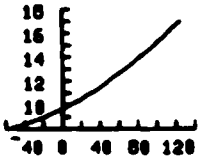
DELAY PATH	LOAD 50 PF 5.5 VOLTS								
	MINIMUM			AVERAGE			MAXIMUM		
	-55 C	25 C	125 C	-55 C	25 C	125 C	-55 C	25 C	125 C
TPD1 CLK-10 500OHM/50PF	7.7	7.5	9.5	7.9	7.9	10.2	8.1	8.3	11.4
TPD0 CLK-10 500OHM/50PF	10.2	10.3	11.7	10.3	10.5	11.9	10.5	10.7	12.2
TPD1 CLK-20 1-300HMXXNTLN	7.0	6.8	9.1	7.2	7.2	9.5	7.4	7.5	10.4
TPD0 CLK-20 1-300HMXXNTLN	10.2	9.8	12.2	11.7	10.4	13.1	13.0	11.0	14.6
THZ OUTPUT CONTROL-30	5.4	5.0	5.0	5.5	5.2	5.2	5.6	5.4	5.6
TLZ OUTPUT CONTROL-30	7.0	7.4	13.2	7.1	7.5	14.1	7.4	8.0	15.5
TZH OUTPUT CONTROL-30	7.9	9.3	16.3	8.0	10.0	17.1	8.1	11.9	18.0
TZL OUTPUT CONTROL-30	9.6	10.4	13.3	9.8	10.6	13.6	10.1	10.8	14.0
TRISE AT 10 500OHM/50PF	1.6	1.7	2.0	1.7	1.8	3.2	1.0	1.9	4.2
TFALL AT 10 500OHM/50PF	1.7	1.7	2.2	1.7	1.8	2.3	1.0	1.9	2.5
TRISE AT 20 1-300HMXXNTLN	1.5	1.5	2.5	1.5	1.7	3.0	1.6	1.0	3.9
TFALL AT 20 1-300HMXXNTLN	1.4	1.4	2.4	1.6	1.7	2.6	1.0	1.0	3.0



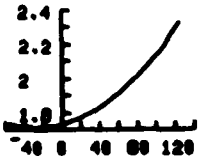
TPD1 CLK-10 500OHM/50PF



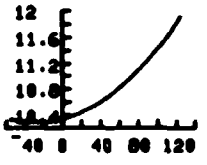
TPD0 CLK-20 1-300HMXXNTLN



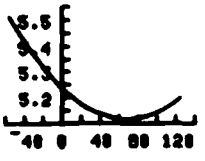
TZH OUTPUT CONTROL-30



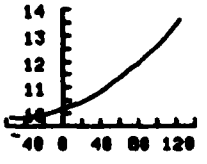
TFALL AT 10 500OHM/50PF



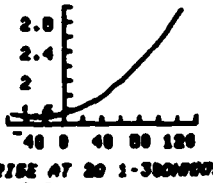
TPD0 CLK-10 500OHM/50PF



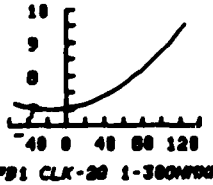
THZ OUTPUT CONTROL-30



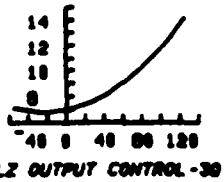
TZL OUTPUT CONTROL-30



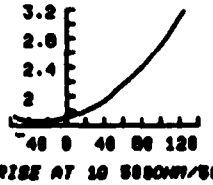
TRISE AT 20 1-300HMXXNTLN



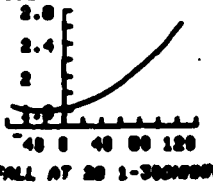
TPD1 CLK-20 1-300HMXXNTLN



TLZ OUTPUT CONTROL-30



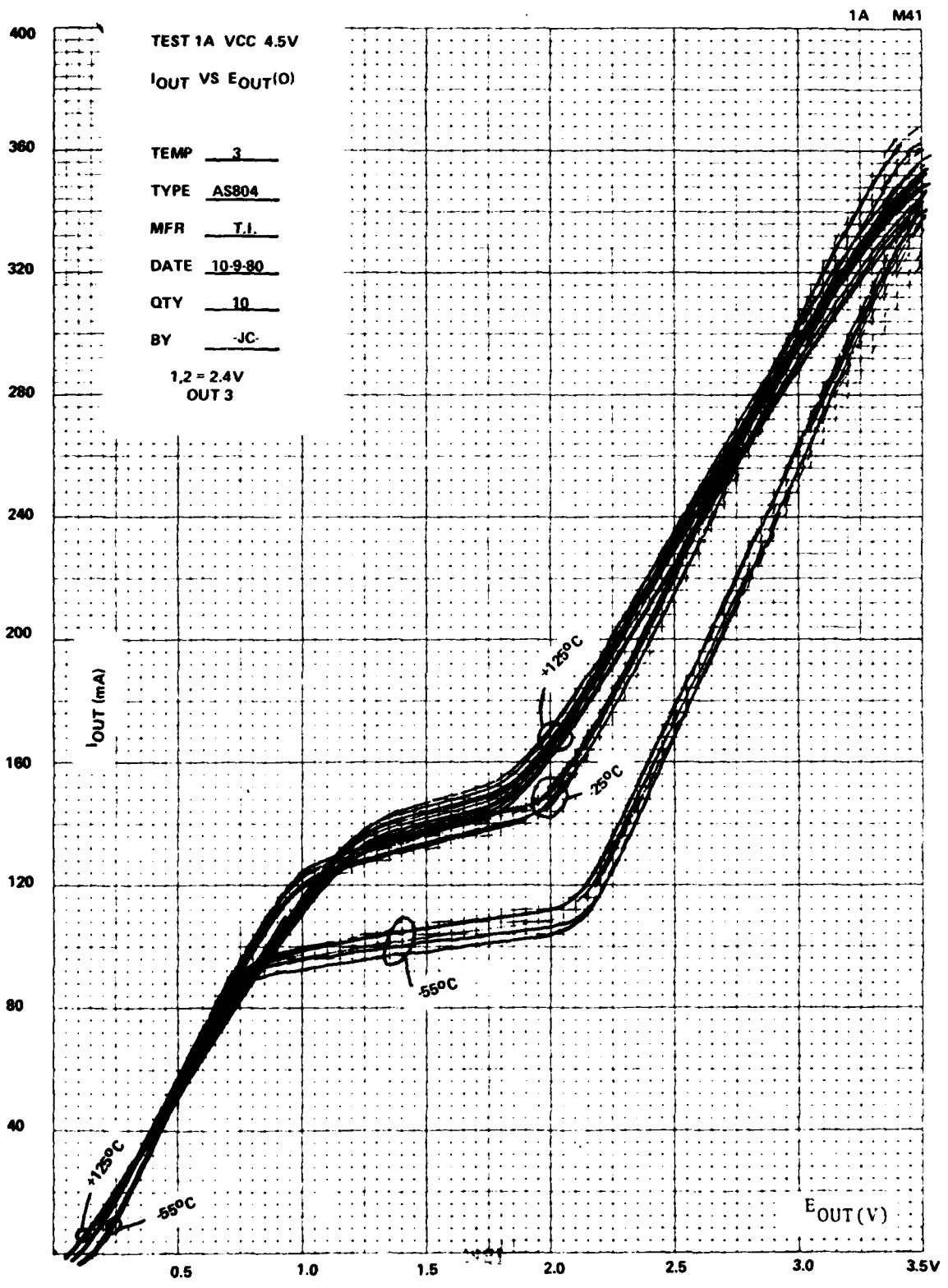
TRISE AT 10 500OHM/50PF

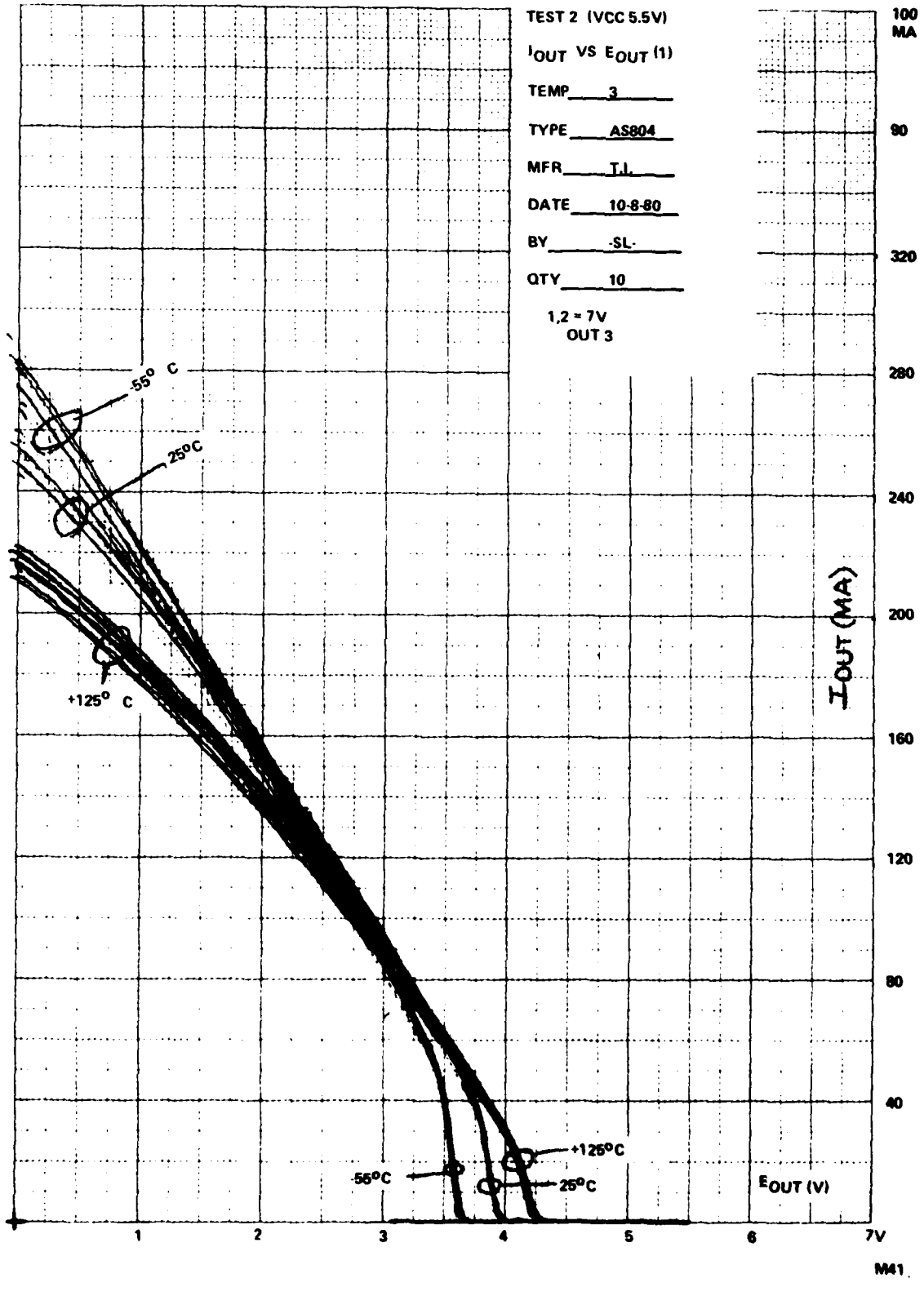


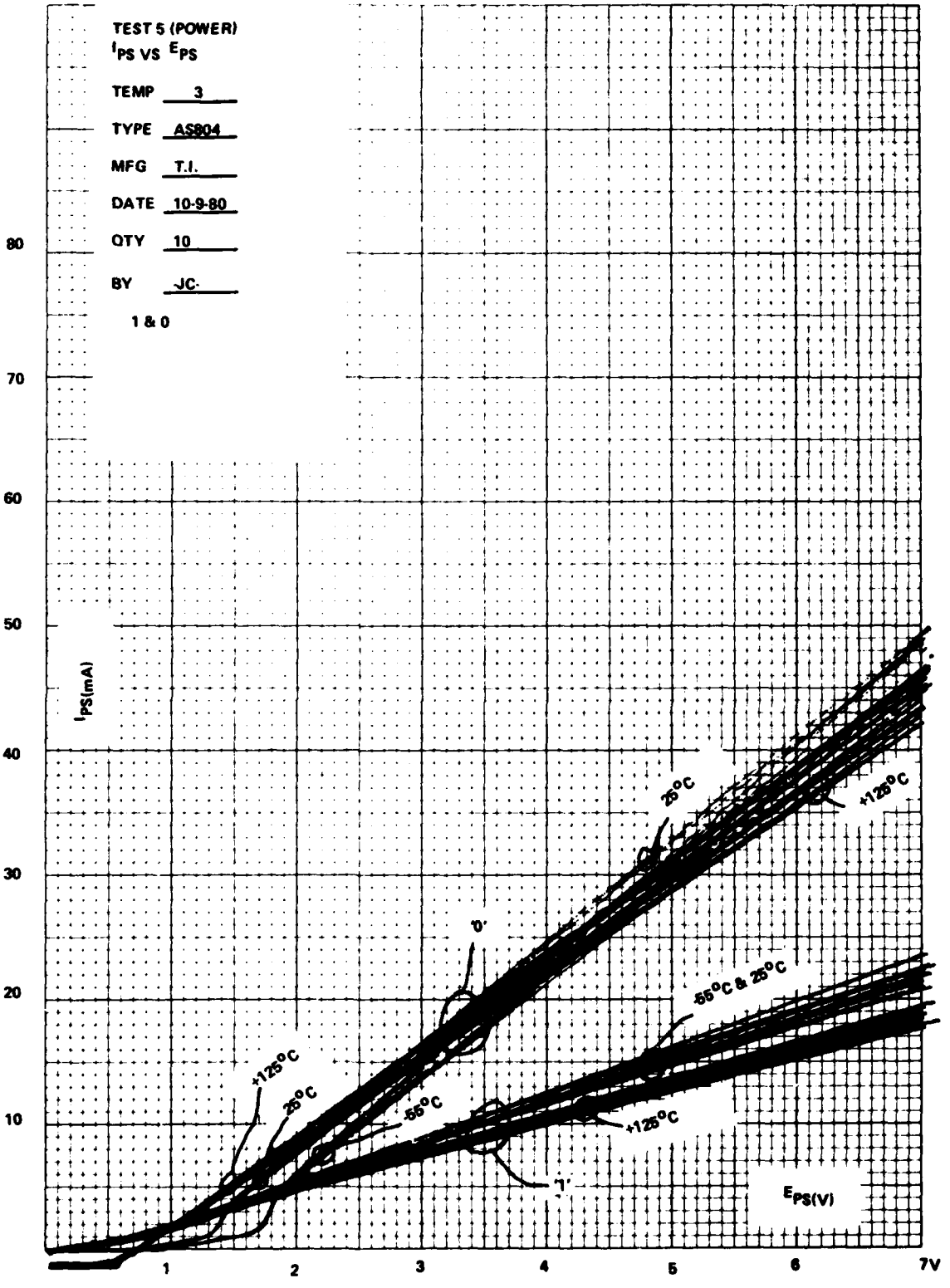
TFALL AT 20 1-300HMXXNTLN

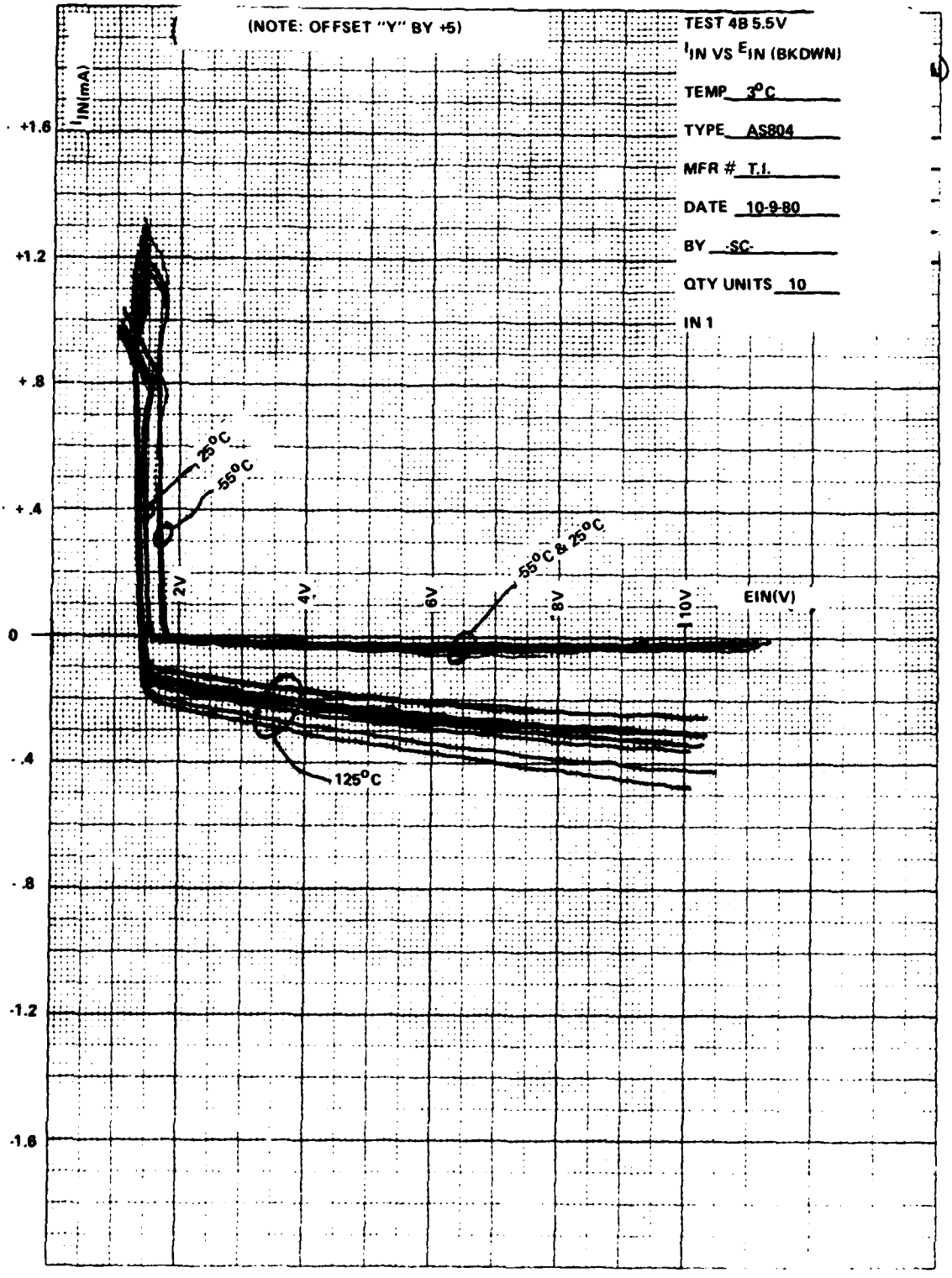
APPENDIX B

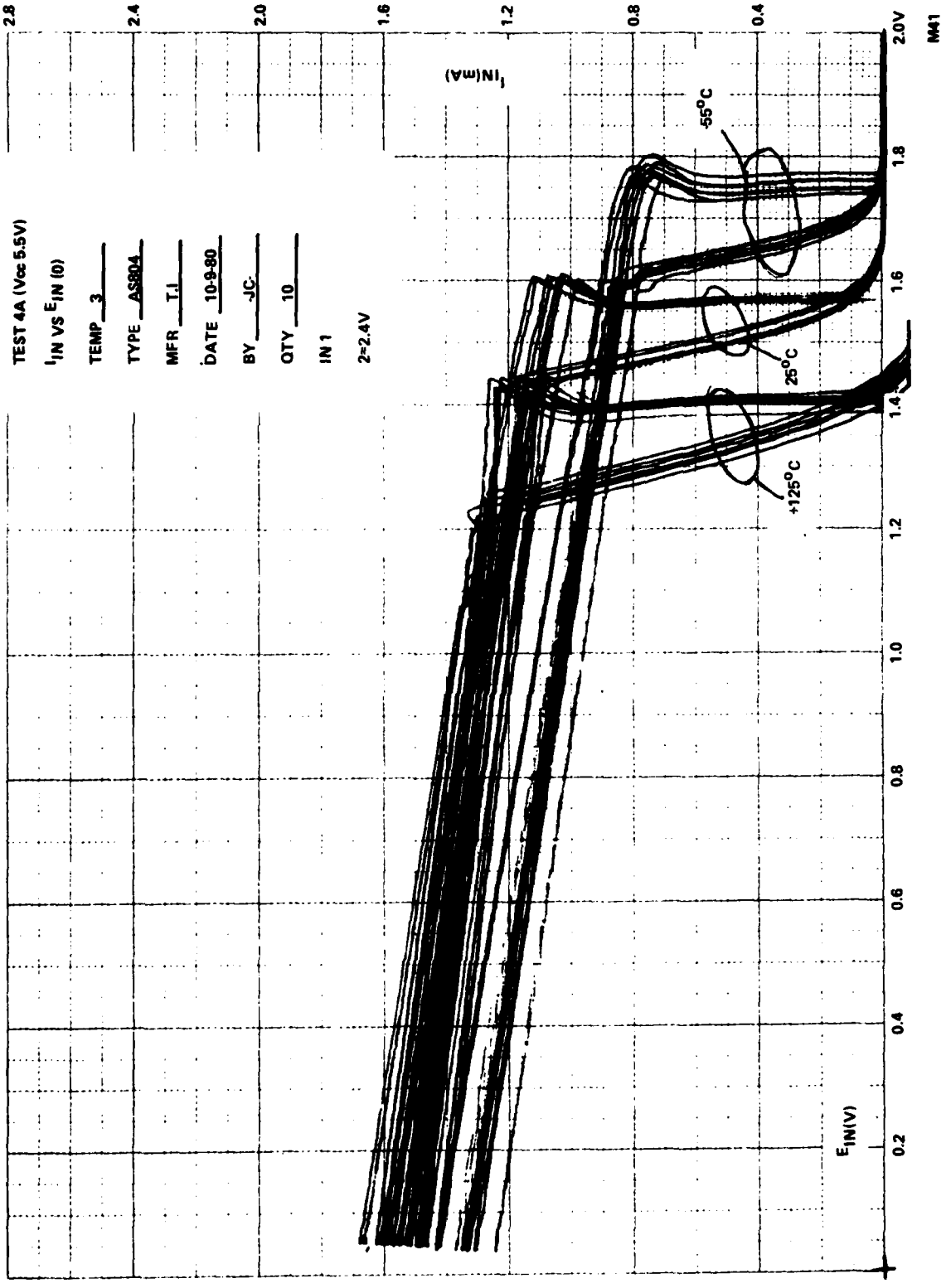
DC CHARACTERIZATION DATA

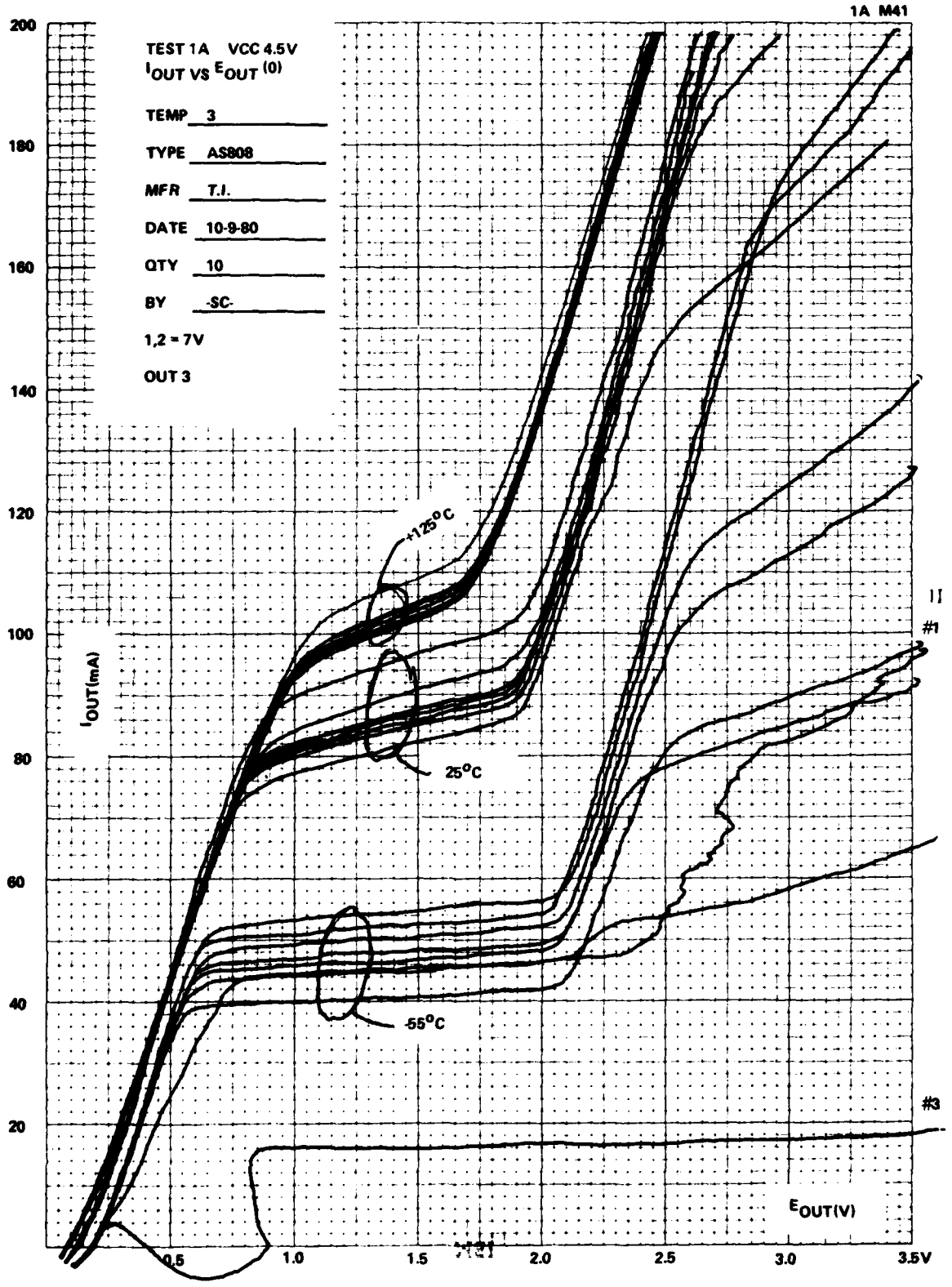

1A M41
TEST 1A VCC 4.5V
I_{OUT} VS E_{OUT}(O)
TEMP 3
TYPE AS804
MFR T.I.
DATE 10-9-80
QTY 10
BY -JC-
1,2 = 2.4V
OUT 3
400
360
320
280
240
200
160
120
80
40
I_{OUT} (mA)
+125°C
-25°C
-55°C
+125°C
-55°C
0.5
1.0
1.5
2.0
2.5
3.0
3.5V
E_{OUT} (V)

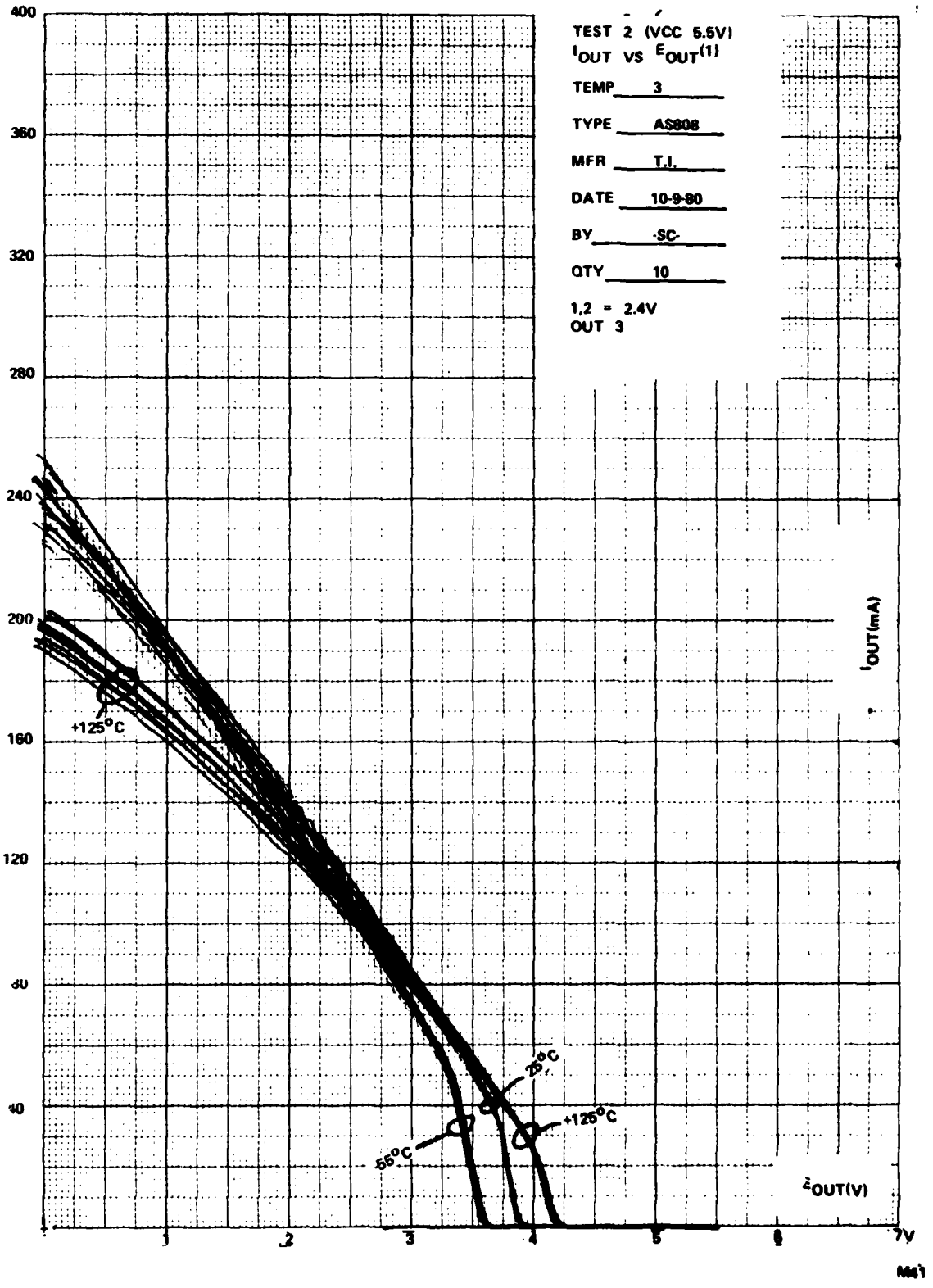

TEST 2 (VCC 5.5V)
I_{OUT} VS E_{OUT} (1)
TEMP 3
TYPE AS804
MFR T.I.
DATE 10-8-80
BY -SL-
QTY 10
1,2 = 7V
OUT 3
-55° C
25°C
+125° C
+125°C
-55°C
25°C
100 MA
90
320
280
240
200
160
120
80
40
I_{OUT} (MA)
E_{OUT} (V)
1
2
3
4
5
6
7V
M41


TEST 5 (POWER)
I_{PS} VS E_{PS}
TEMP 3
TYPE AS804
MFG T.I.
DATE 10-9-80
QTY 10
BY JC
1 & 0
80
70
60
50
40
30
20
10
$I_{PS(mA)}$
'0'
'1'
+125°C
25°C
-55°C
-55°C & 25°C
+125°C
25°C
+125°C
$E_{PS(V)}$
1
2
3
4
5
6
7V

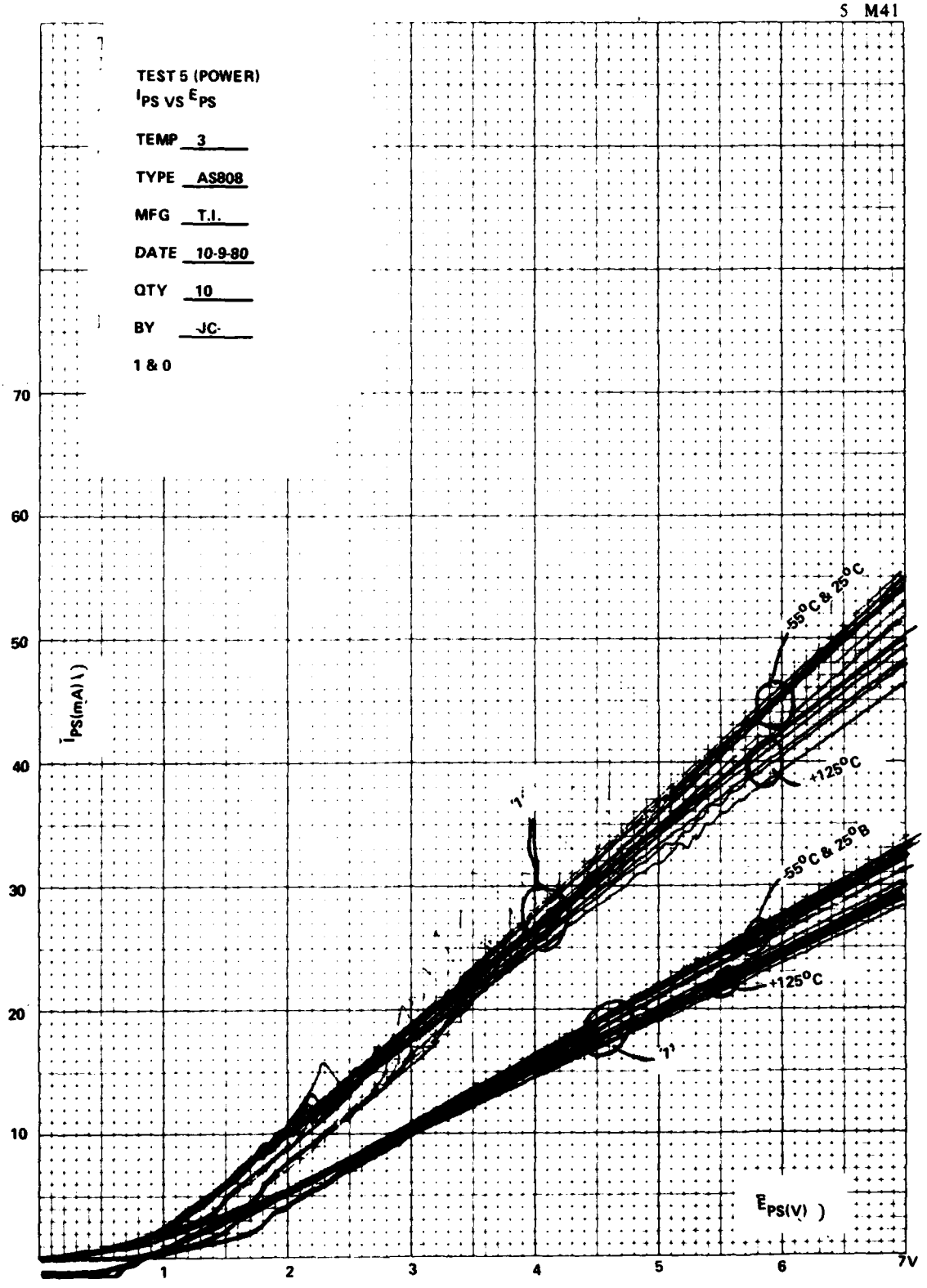

(NOTE: OFFSET "Y" BY +5)
TEST 4B 5.5V
I_{IN} VS E_{IN} (BKDWN)
TEMP 3°C
TYPE AS804
MFR # T.I.
DATE 10-9-80
BY SC
QTY UNITS 10
IN 1
I_{IN}(mA)
+1.6
+1.2
+.8
+.4
0
-.4
-.8
-1.2
-1.6
2V
4V
6V
8V
10V
EIN(V)
25°C
55°C
-55°C & 25°C
125°C

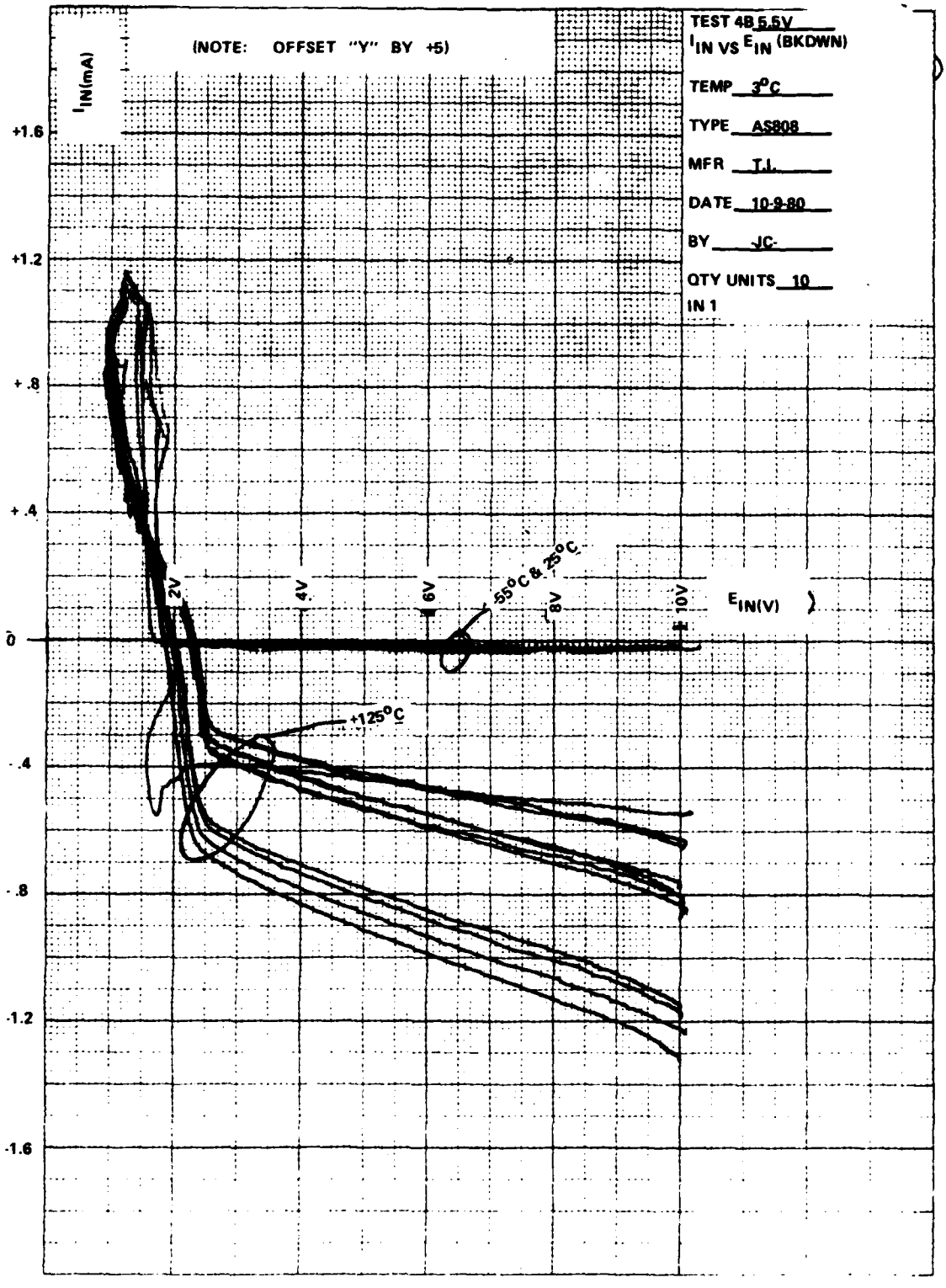

TEST 4A (Vcc 5.5V)
I_{IN} VS E_{IN} (0)
TEMP 3
TYPE AS804
MFR T.I
DATE 10-9-80
BY JC
QTY 10
IN 1
2=2.4V
I_{IN}(mA)
E_{IN}(V)
-55°C
25°C
+125°C
M41

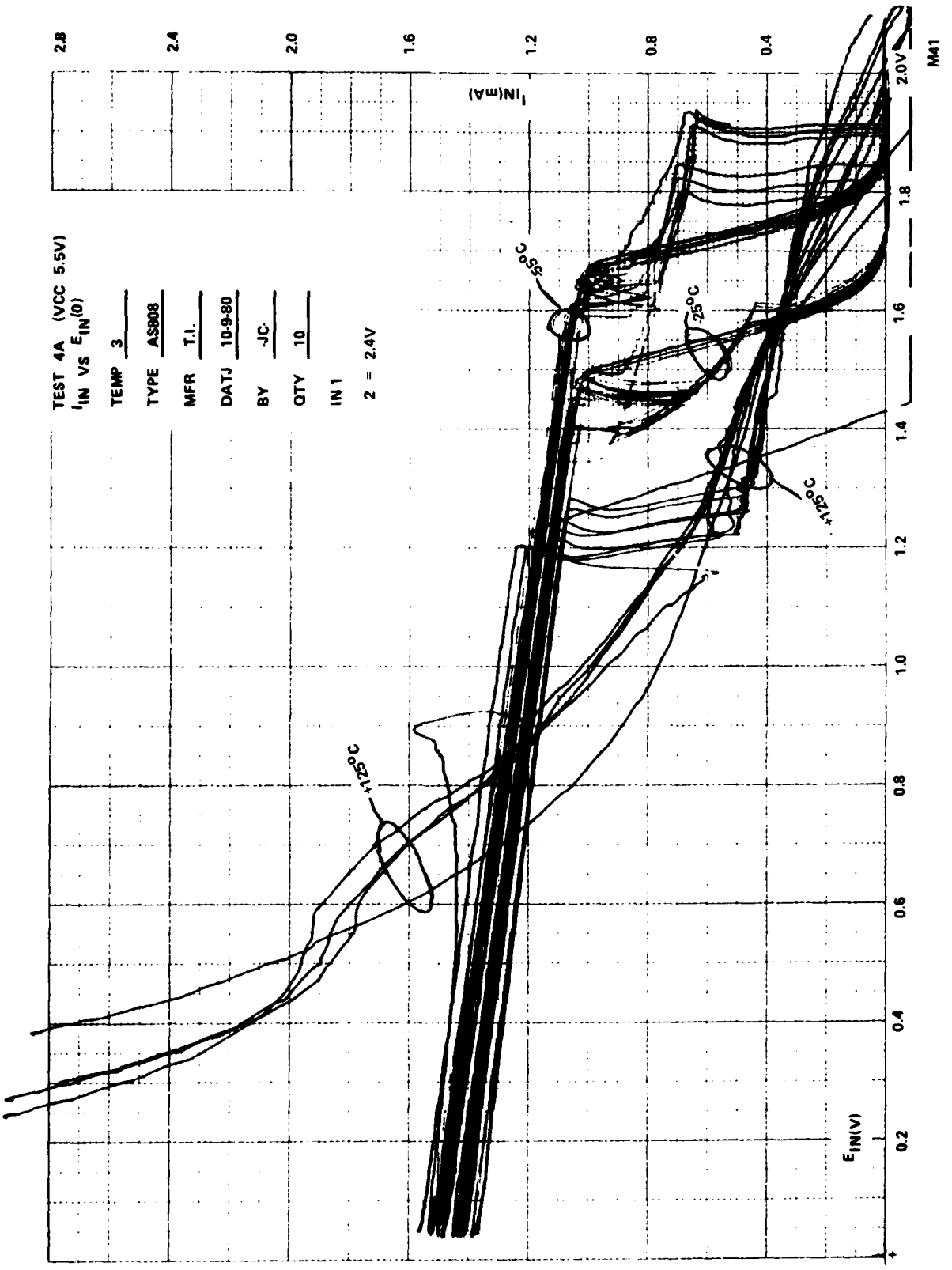

1A M41
TEST 1A VCC 4.5V
I_{OUT} VS E_{OUT} (0)
TEMP 3
TYPE AS808
MFR T.I.
DATE 10-9-80
QTY 10
BY -SC-
1,2 = 7V
OUT 3
200
180
160
140
120
100
80
60
40
20
I_{OUT}(mA)
+125°C
25°C
-55°C
#1
#3
0.5
1.0
1.5
2.0
2.5
3.0
3.5V
E_{OUT}(V)

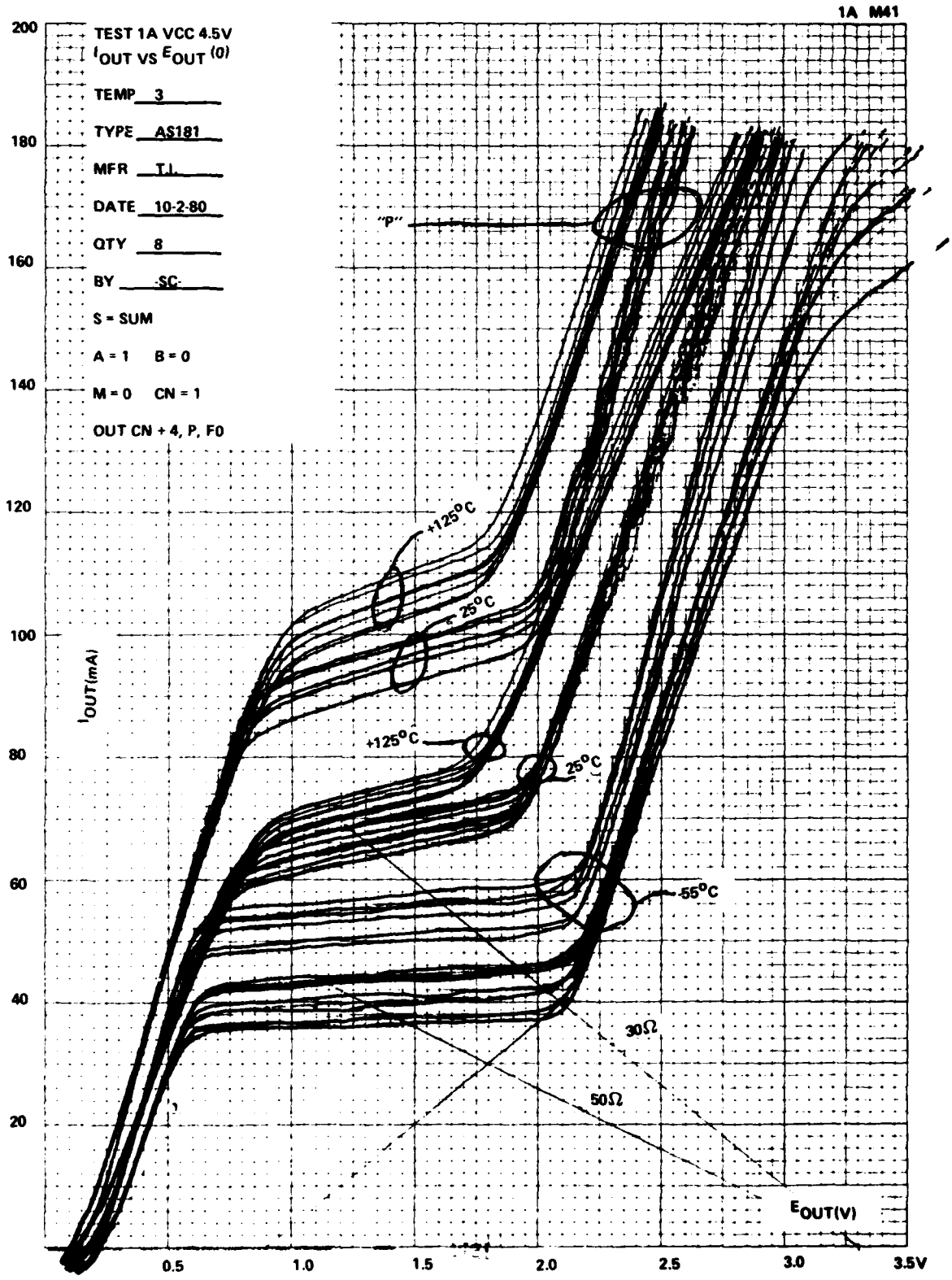

TEST 2 (VCC 5.5V)
I_{OUT} VS $E_{OUT}(1)$
TEMP 3
TYPE AS808
MFR T.I.
DATE 10-9-80
BY SC
QTY 10
1,2 = 2.4V
OUT 3
400
360
320
280
240
200
160
120
80
40
I_{OUT}(mA)
+125°C
25°C
+125°C
-55°C
E_{OUT}(V)
1
2
3
4
5
6
7V
M41

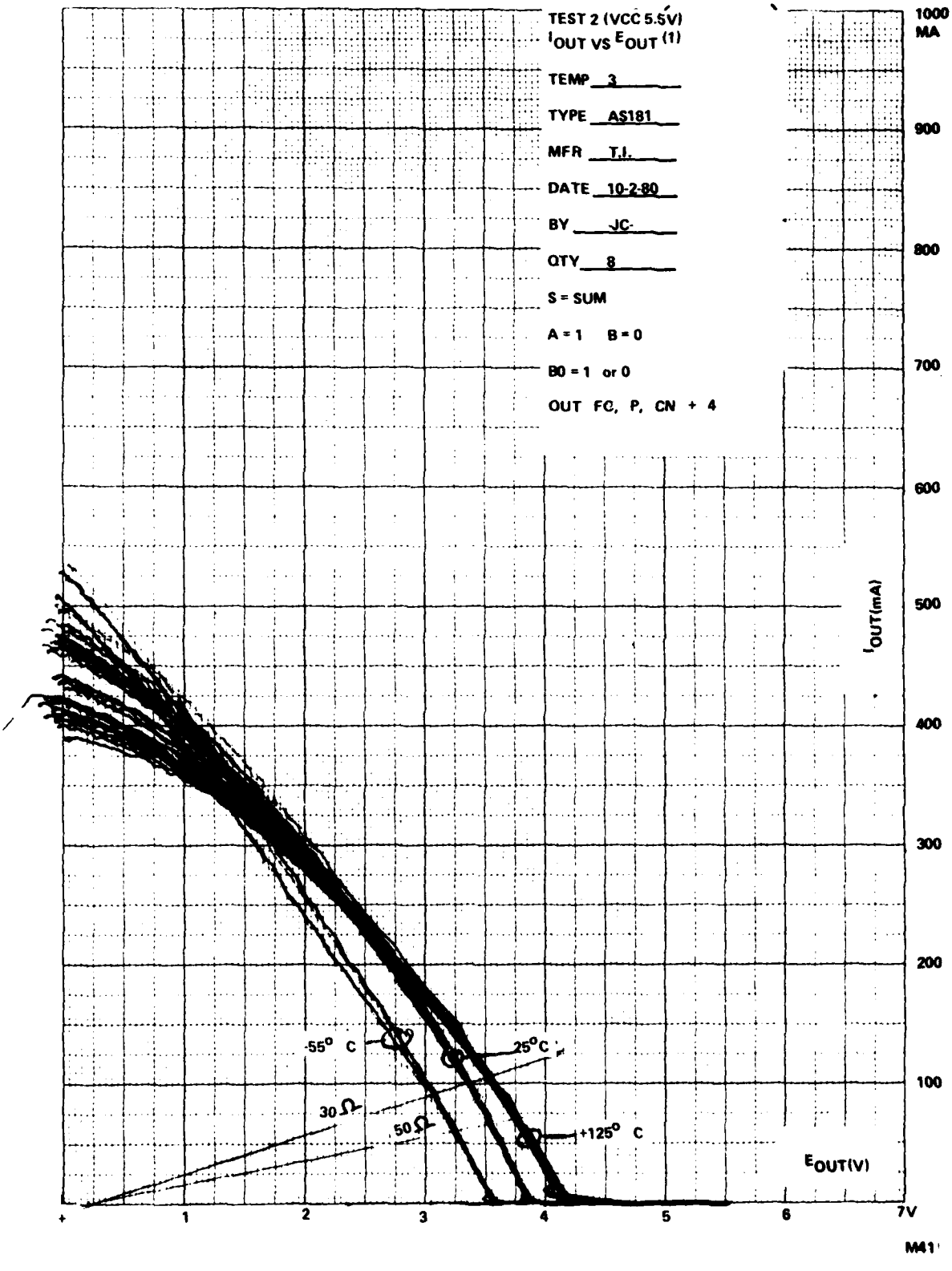
5 M41

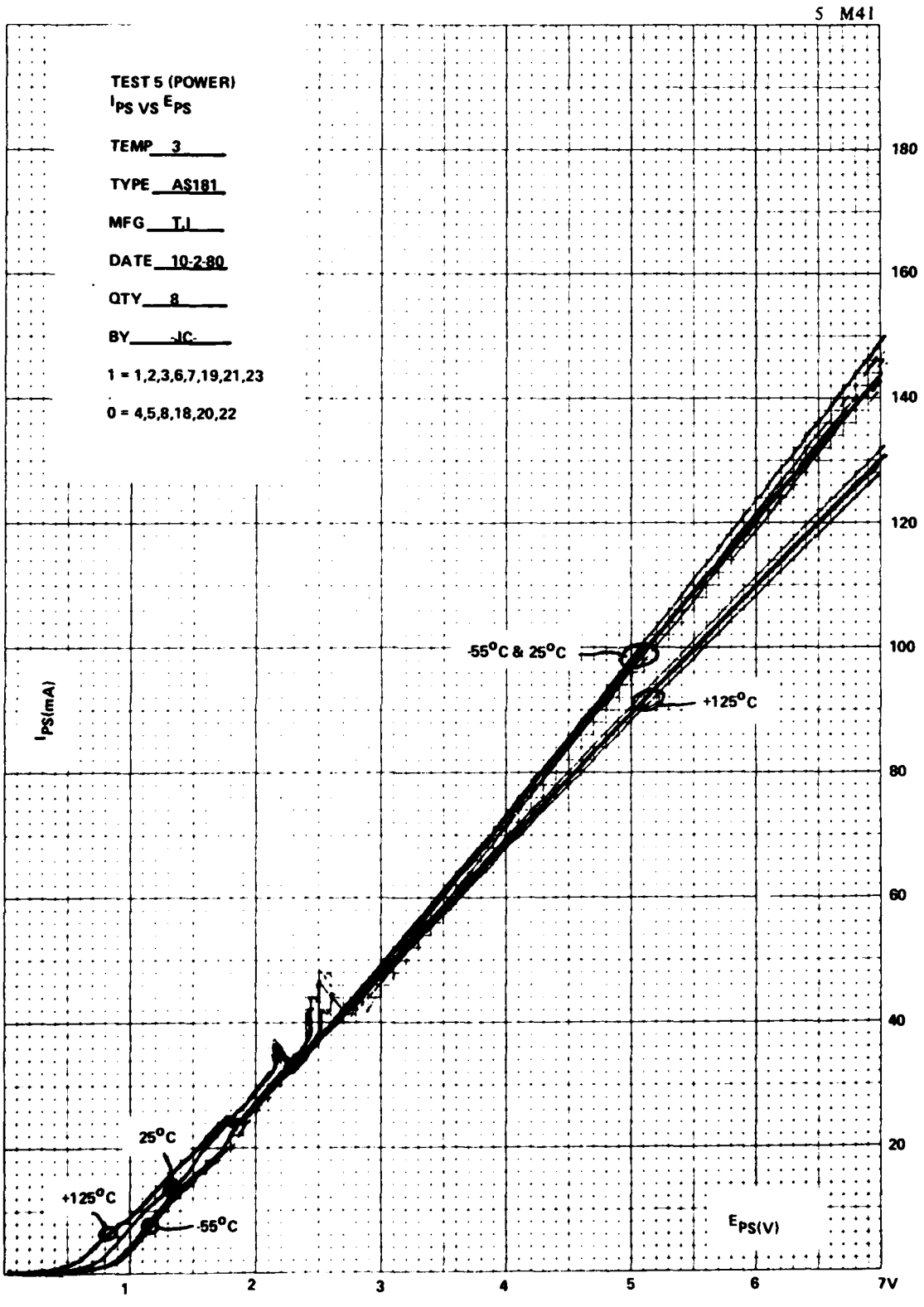

TEST 5 (POWER)
I_{PS} VS E_{PS}
TEMP 3
TYPE AS808
MFG T.I.
DATE 10-9-80
QTY 10
BY JC
1 & 0
70
60
50
40
30
20
10
$I_{PS(mA)}$)
-55°C & 25°C
+125°C
'1'
-55°C & 25°C
+125°C
'1'
$E_{PS(V)}$)
1
2
3
4
5
6
7V

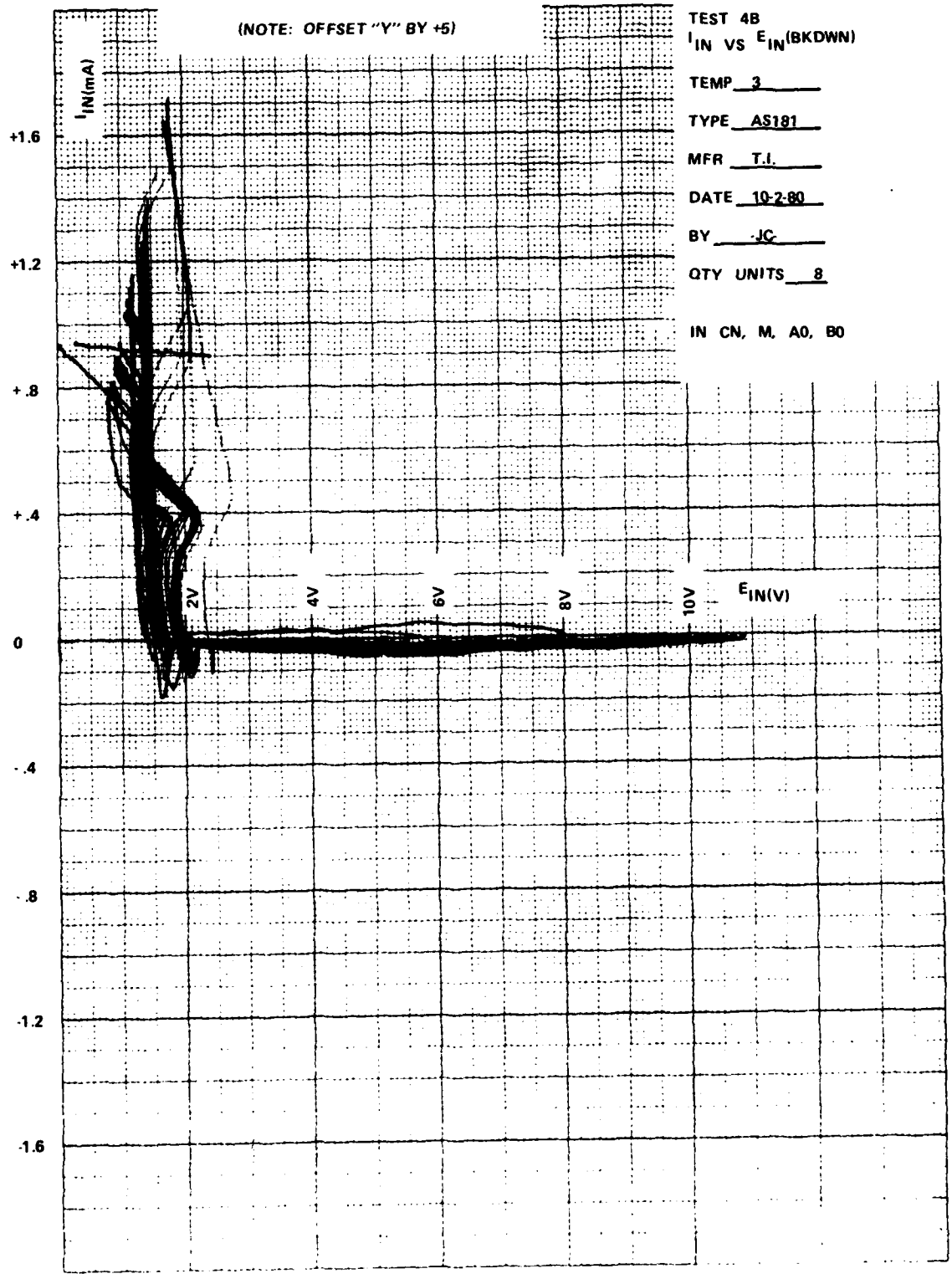

(NOTE: OFFSET "Y" BY +5)
$I_{IN(mA)}$
TEST 4B 5.5V
I_{IN} VS E_{IN} (BKDWN)
TEMP 3°C
TYPE AS808
MFR T.I.
DATE 10-9-80
BY JC
QTY UNITS 10
IN 1
+1.6
+1.2
+.8
+.4
0
-.4
-.8
-1.2
-1.6
2V
4V
6V
8V
10V
$E_{IN(V)}$
-55°C & 25°C
+125°C

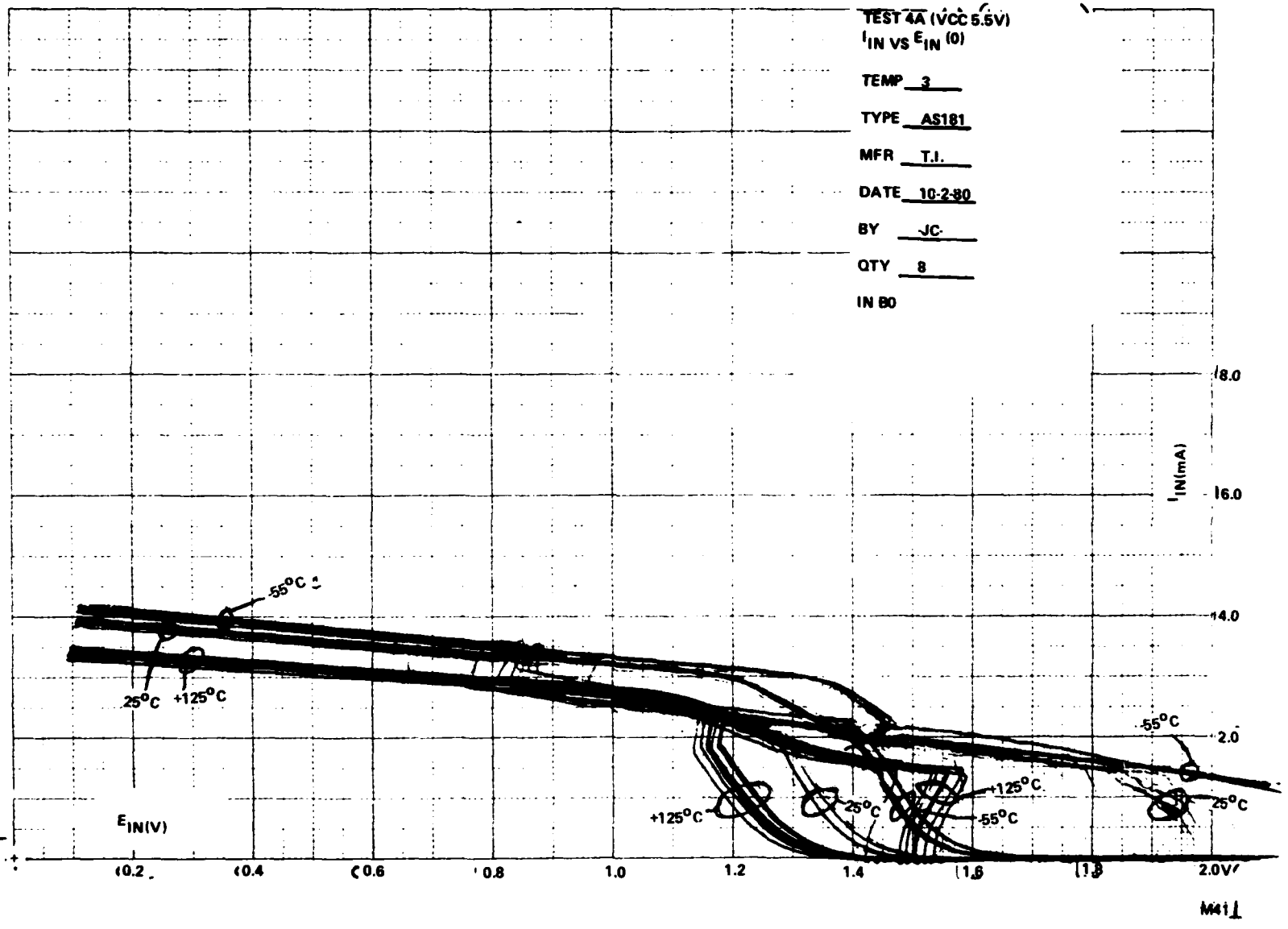

TEST 4A (VCC 5.5V)
I_{IN} VS $E_{IN}(0)$
TEMP 3
TYPE AS808
MFR T.I.
DATJ 10-9-80
BY -JC-
QTY 10
IN 1
2 = 2.4V
I_{IN}(mA)
E_{IN}(V)
-55°C
25°C
+125°C
+125°C
M41

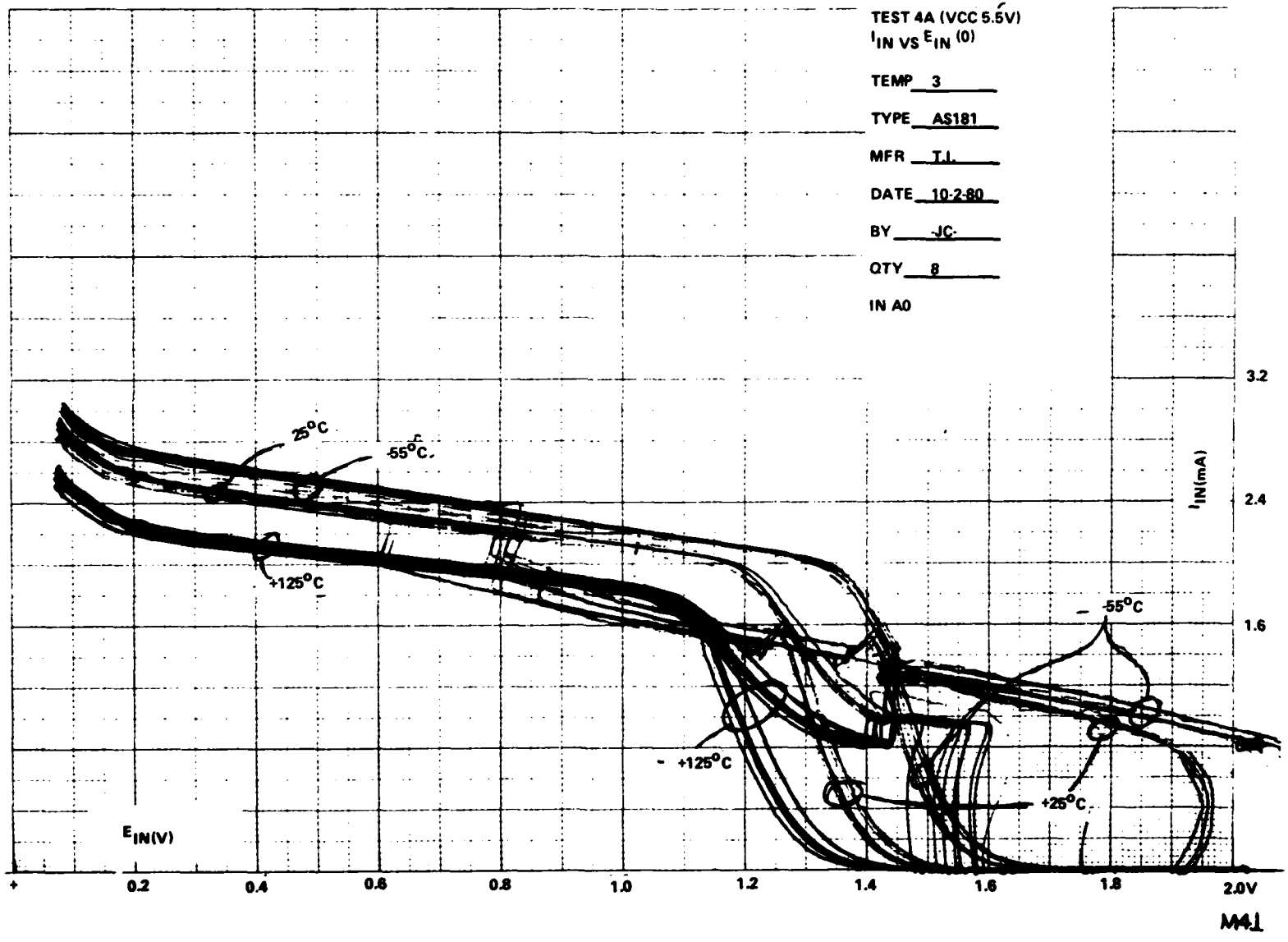

1A M41
TEST 1A VCC 4.5V
I_{OUT} VS E_{OUT} (0)
TEMP 3
TYPE AS181
MFR T.I.
DATE 10-2-80
QTY 8
BY SC
S = SUM
A = 1 B = 0
M = 0 CN = 1
OUT CN + 4, P, F0
"P"
+125°C
25°C
+125°C
25°C
-55°C
30Ω
50Ω
I_{OUT}(mA)
E_{OUT}(V)
200
180
160
140
120
100
80
60
40
20
0.5
1.0
1.5
2.0
2.5
3.0
3.5V

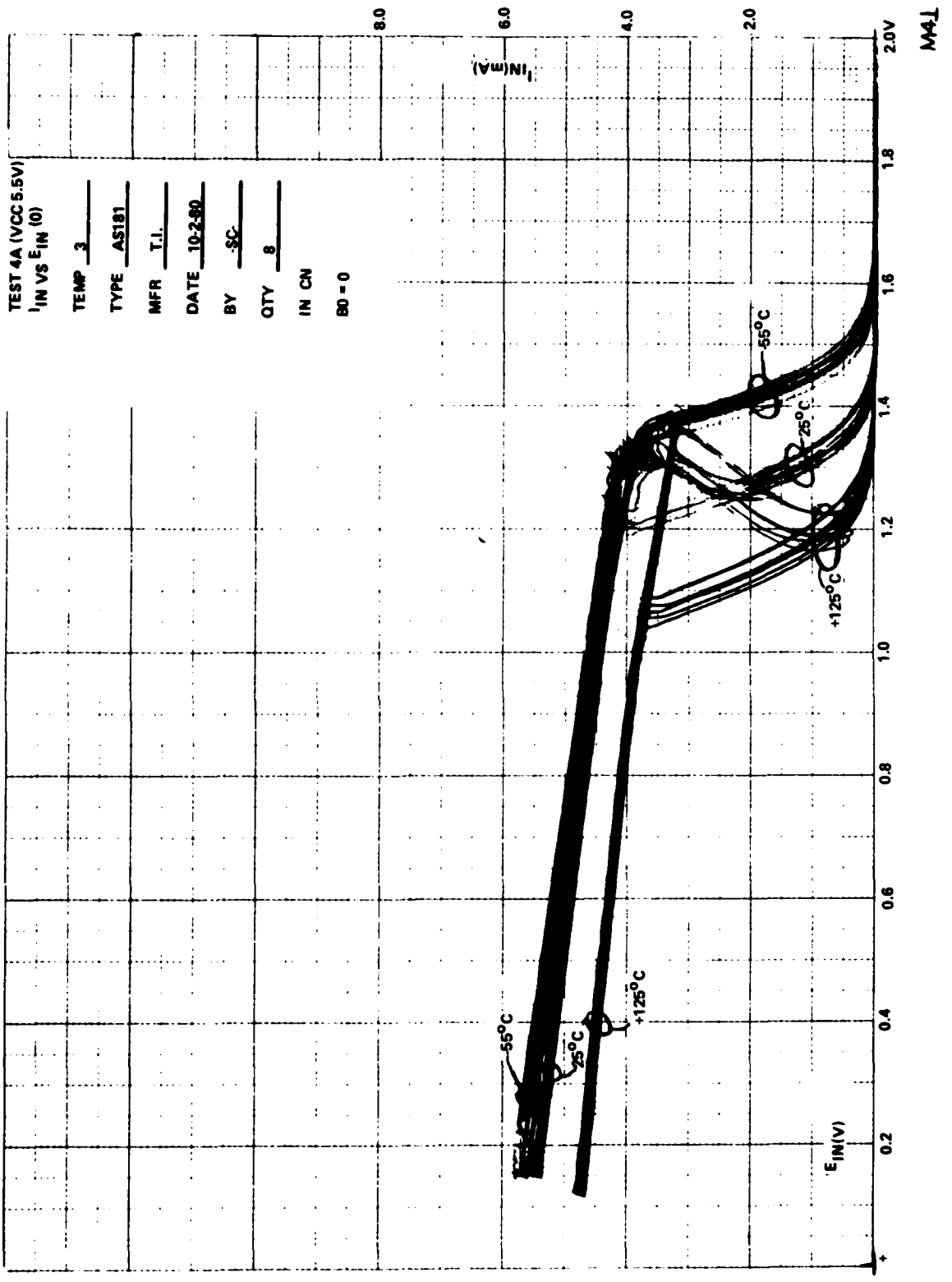

TEST 2 (VCC 5.5V)
I_{OUT} VS E_{OUT} (1)
TEMP 3
TYPE AS181
MFR T.I.
DATE 10-2-80
BY JC
QTY 8
S = SUM
A = 1 B = 0
B0 = 1 or 0
OUT FC, P, CN + 4
1000 MA
900
800
700
600
500
400
300
200
100
I_{OUT}(mA)
-55° C
25° C
+125° C
30Ω
50Ω
E_{OUT}(V)
+
1
2
3
4
5
6
7V
M41

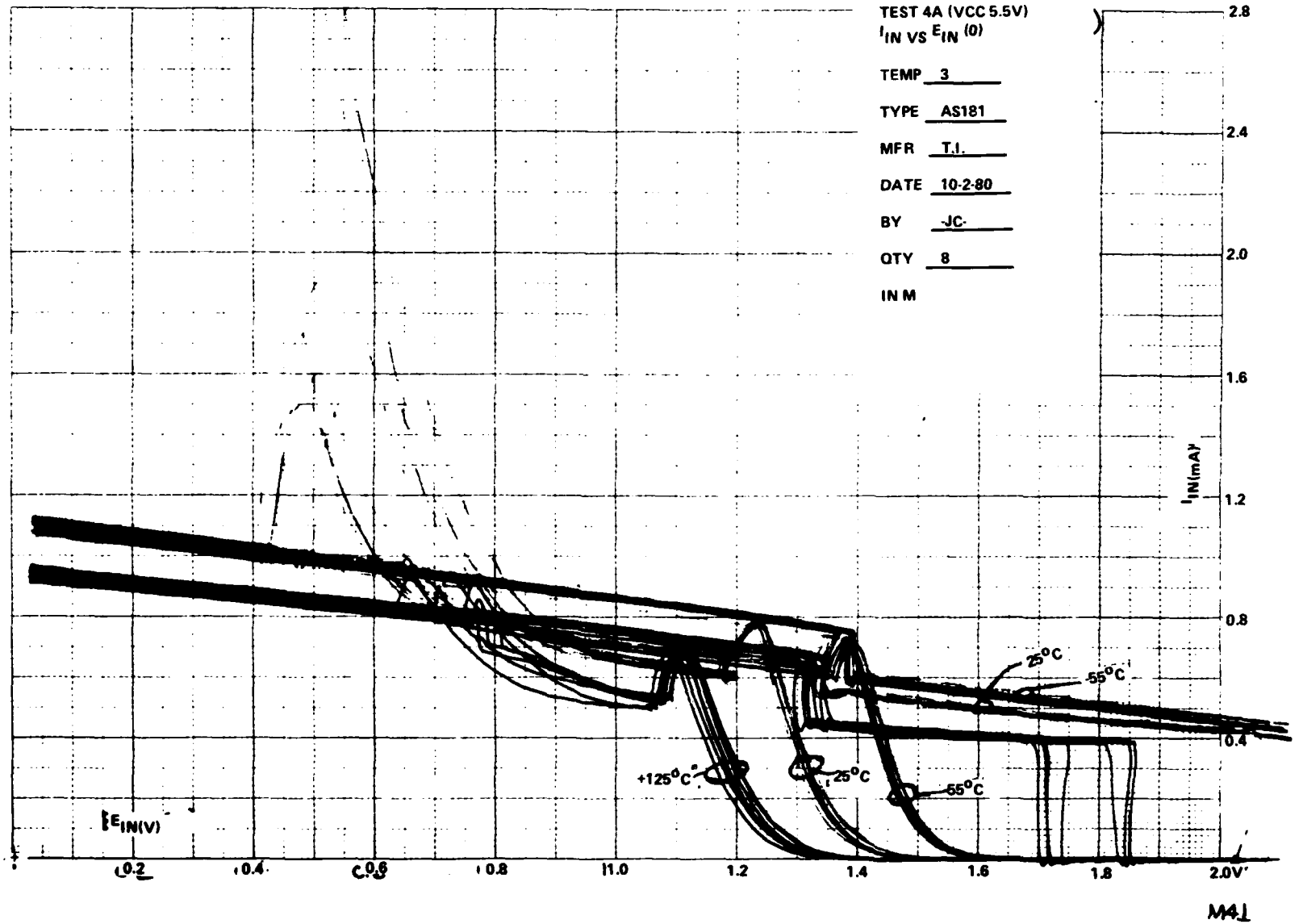

5 M41
TEST 5 (POWER)
I_{PS} VS E_{PS}
TEMP 3
TYPE AS181
MFG T.I
DATE 10-2-80
QTY 8
BY JC
1 = 1,2,3,6,7,19,21,23
0 = 4,5,8,18,20,22
$I_{PS(mA)}$
$E_{PS(V)}$
-55°C & 25°C
+125°C
25°C
+125°C
-55°C
180
160
140
120
100
80
60
40
20
1
2
3
4
5
6
7V

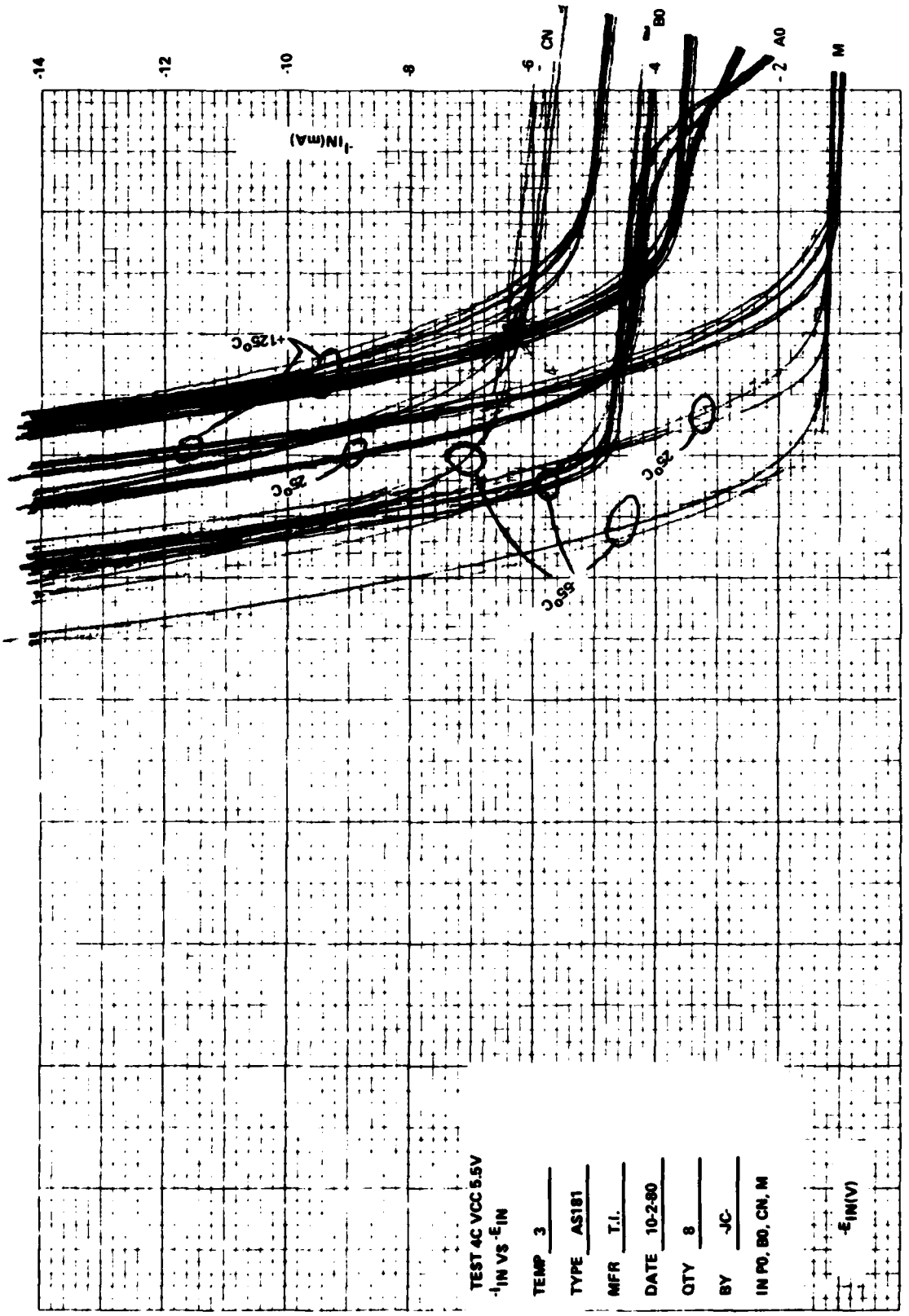

(NOTE: OFFSET "Y" BY +5)
TEST 4B
I_{IN} VS E_{IN}(BKDWN)
TEMP 3
TYPE AS181
MFR T.I.
DATE 10-2-80
BY JC
QTY UNITS 8
IN CN, M, A0, B0
I_{IN}(mA)
+1.6
+1.2
+.8
+.4
0
-.4
-.8
-1.2
-1.6
2V
4V
6V
8V
10V
E_{IN}(V)

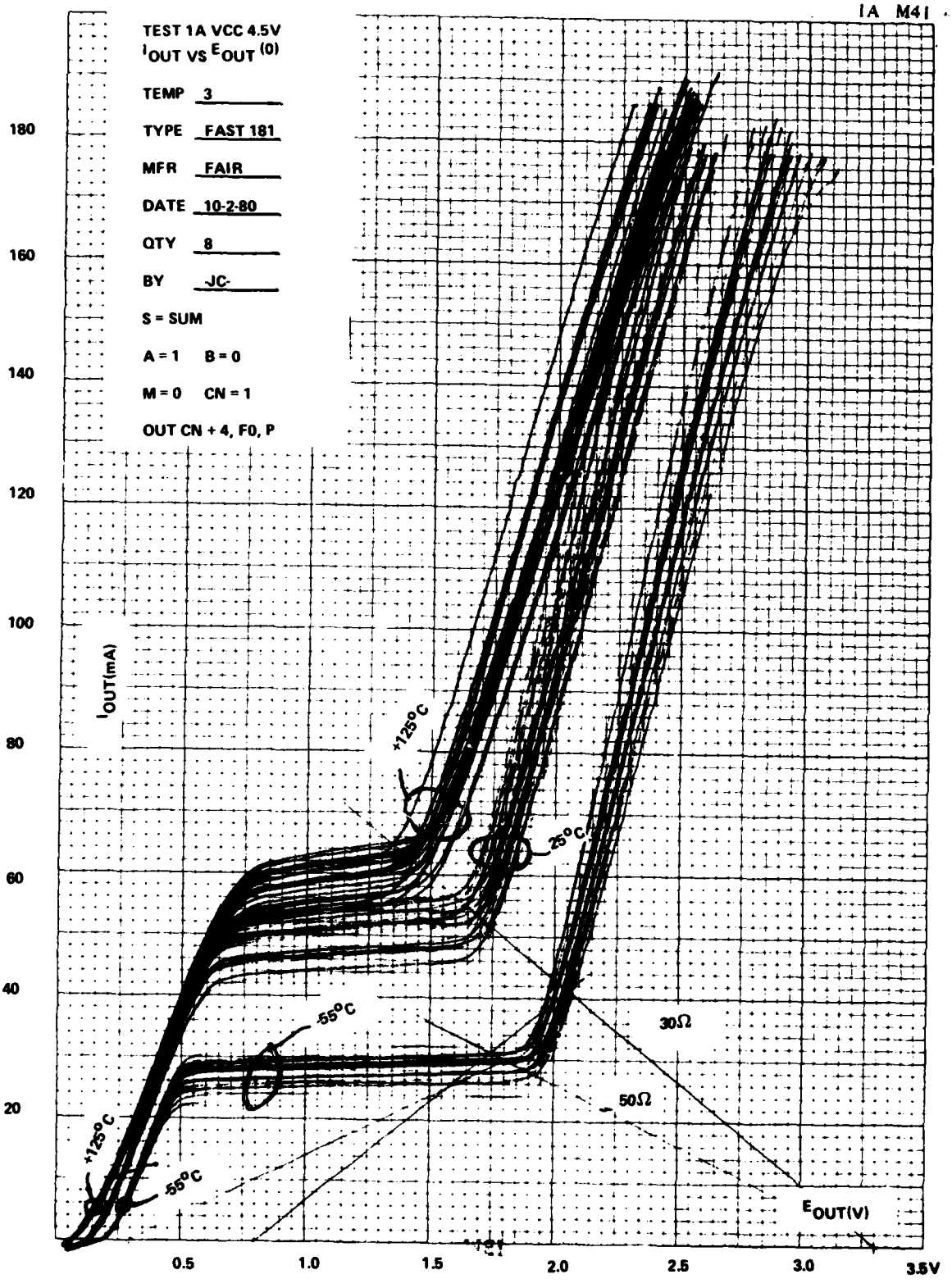

TEST 4A (VCC 5.5V)
I_{IN} VS E_{IN} (0)
TEMP 3
TYPE AS181
MFR T.I.
DATE 10-2-80
BY JC
QTY 8
IN B0
I_{IN}(mA)
18.0
16.0
14.0
2.0
E_{IN}(V)
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0V
-55°C
25°C
+125°C
+125°C
25°C
-55°C
+125°C
25°C
-55°C
M41

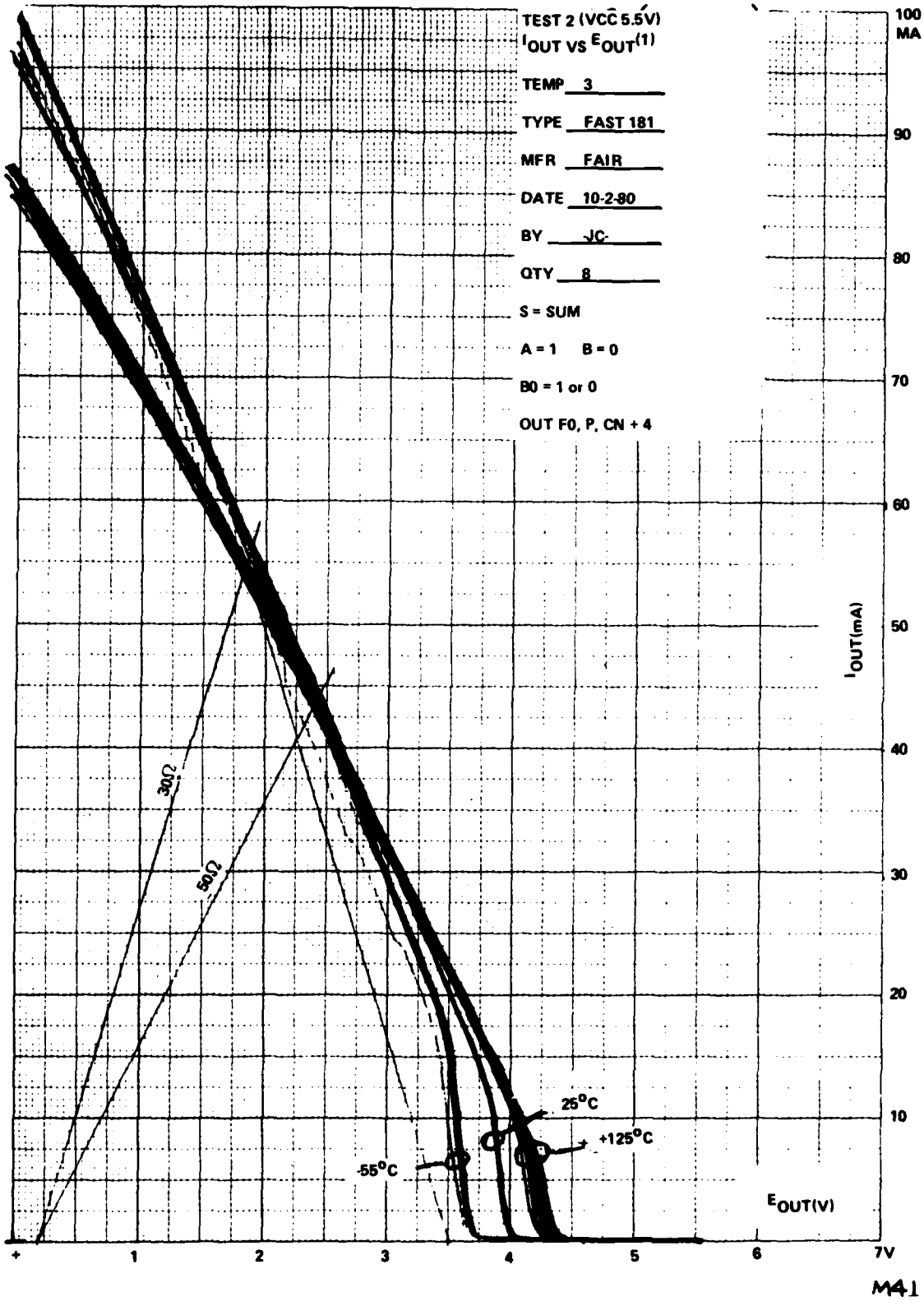

TEST 4A (VCC 5.5V)
I_{IN} VS E_{IN} (0)
TEMP 3
TYPE AS181
MFR T.I.
DATE 10-2-80
BY JC
QTY 8
IN A0
25°C
-55°C
+125°C
-55°C
+125°C
+25°C
$E_{IN(V)}$
$I_{IN(mA)}$
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0V
3.2
2.4
1.6
M41

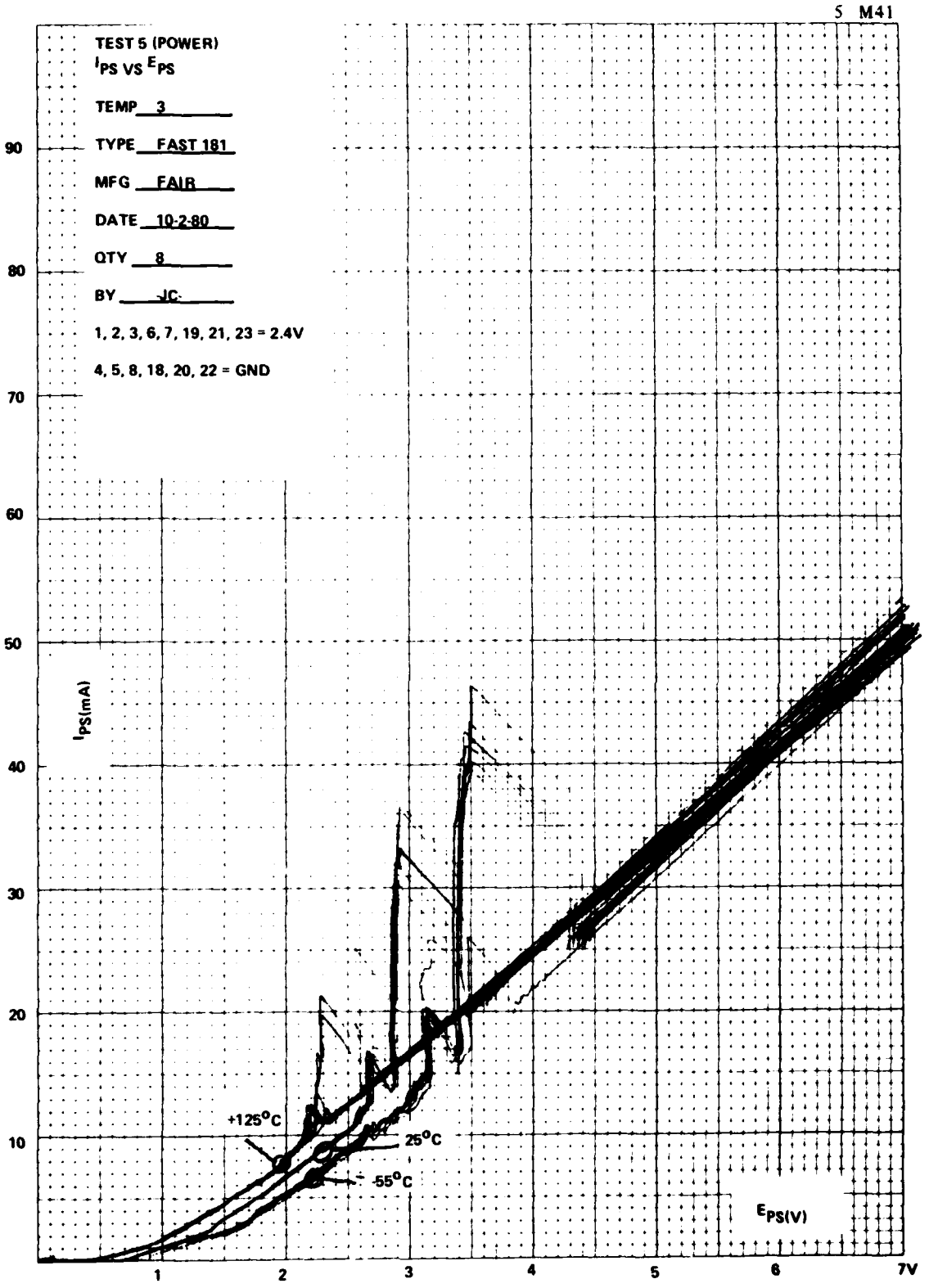

TEST 4A (VCC 5.5V)
I_{IN} VS E_{IN} (0)
TEMP 3
TYPE AS181
MFR T.I.
DATE 10-2-80
BY SC
QTY 8
IN CN
BD = 0
I_{IN}(mA)
8.0
6.0
4.0
2.0
E_{IN}(V)
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0V
-55°C
25°C
+125°C
-55°C
25°C
+125°C
M4L

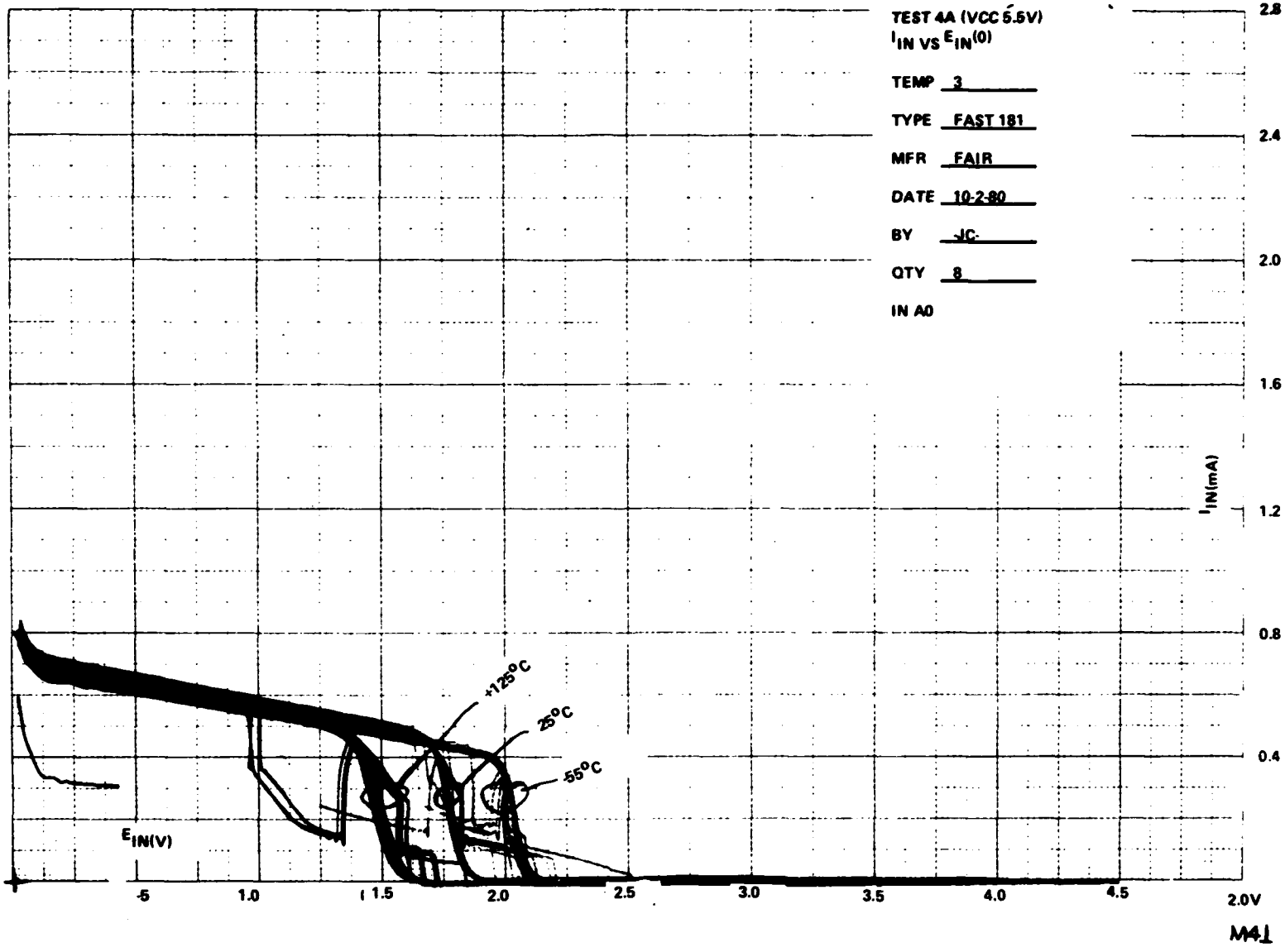

TEST 4A (VCC 5.5V)
I_{IN} VS E_{IN} (0)
TEMP 3
TYPE AS181
MFR T.I.
DATE 10-2-80
BY JC
QTY 8
IN M
2.8
2.4
2.0
1.6
1.2
0.8
0.4
$I_{IN(mA)}$
25°C
55°C
+125°C
25°C
55°C
$E_{IN(V)}$
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0V
M41

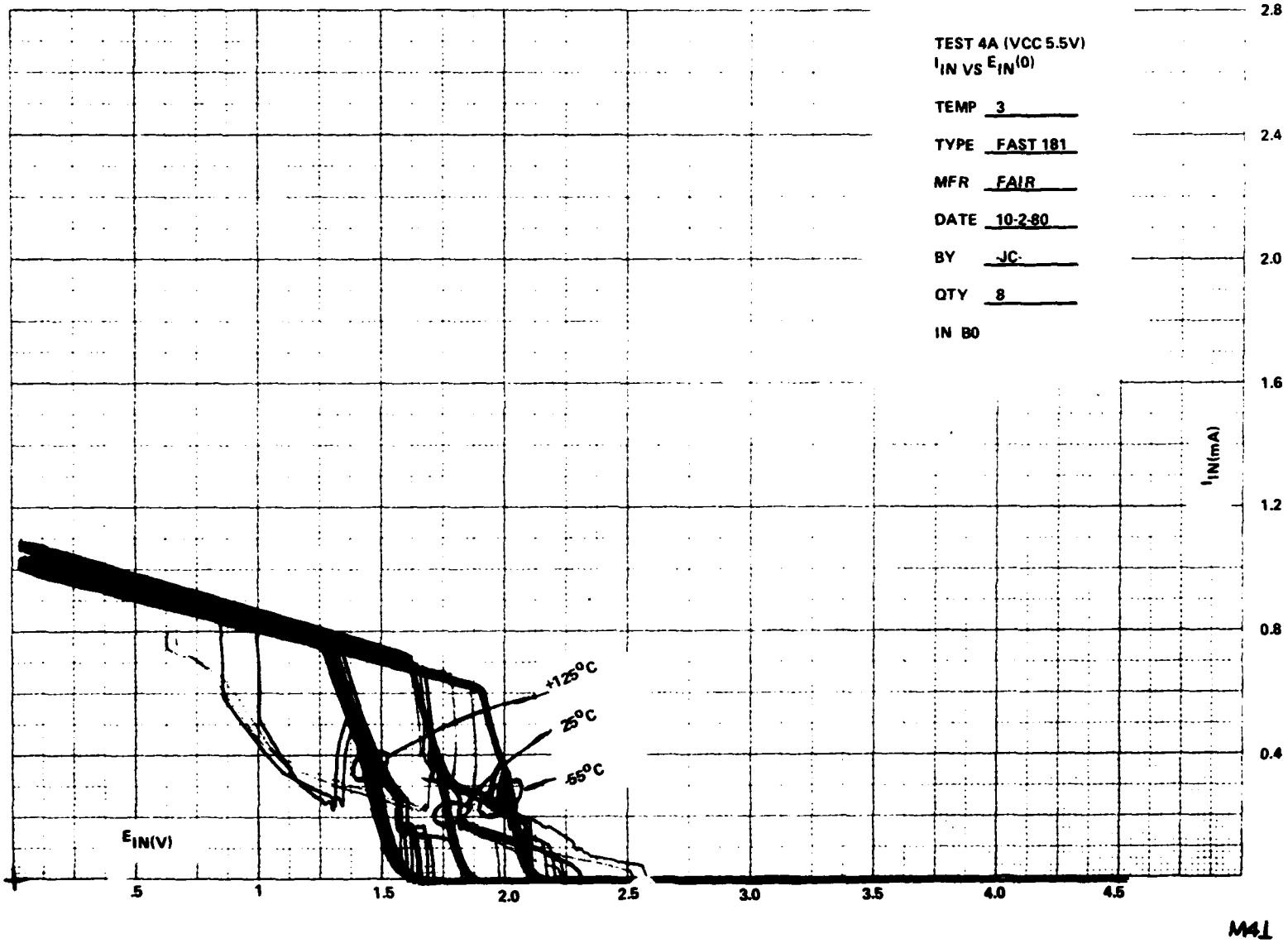

-I_IN(mA)
-14
-12
-10
-8
-6
-4
-2
CN
BD
AD
M
+125°C
25°C
-55°C
-0.2
-0.4
-0.6
-0.8
-1.0
-1.2
-1.4
-1.6
-1.8
-2.0
-E_IN(V)
TEST 4C VCC 5.5V
-I_IN VS -E_IN
TEMP 3
TYPE AS181
MFR T.I.
DATE 10-2-80
QTY 8
BY JC
IN PD, BD, CN, M

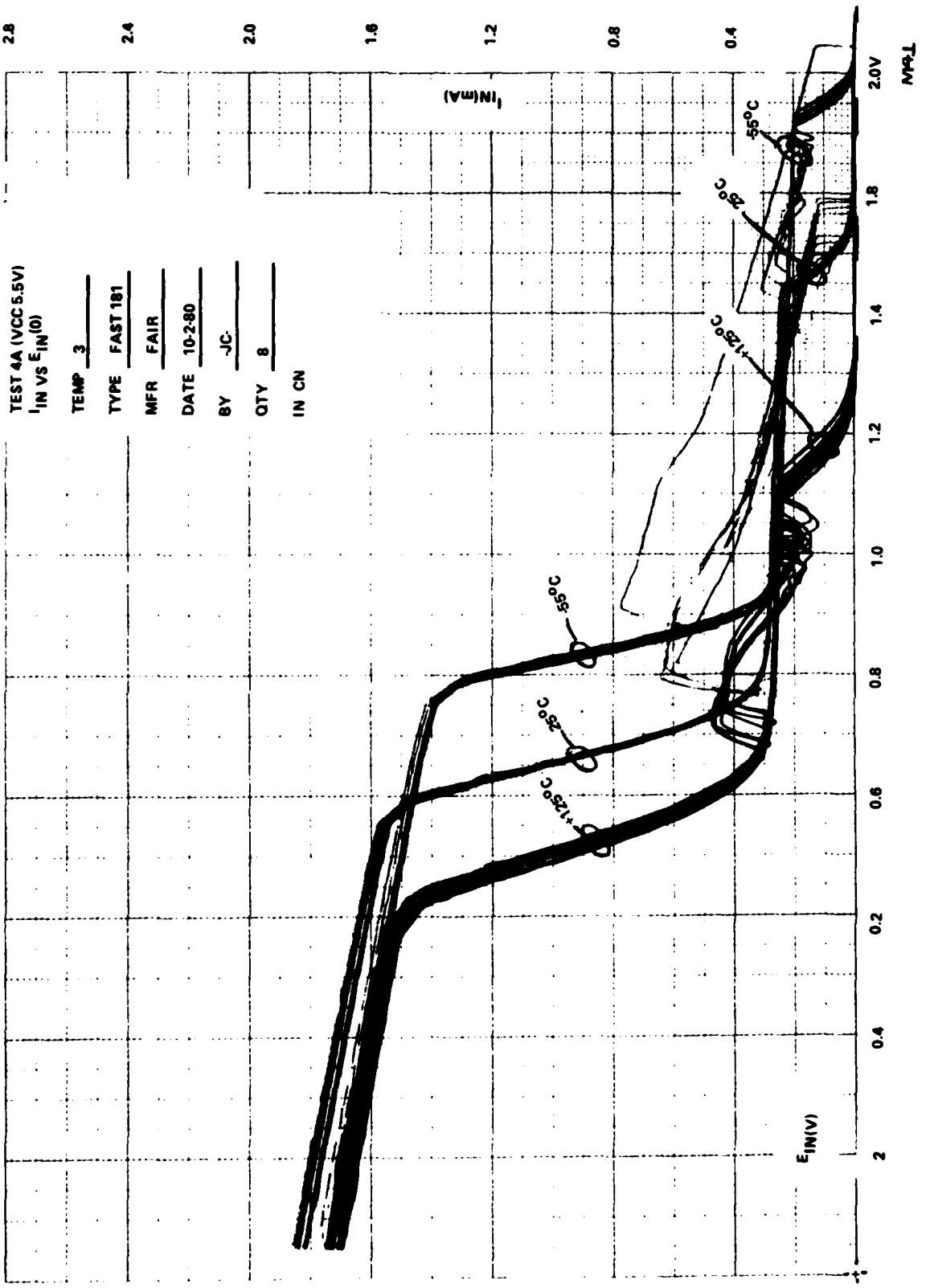

TEST 1A VCC 4.5V
I_{OUT} VS E_{OUT} (0)
TEMP 3
TYPE FAST 181
MFR FAIR
DATE 10-2-80
QTY 8
BY JC
S = SUM
A = 1 B = 0
M = 0 CN = 1
OUT CN + 4, F0, P
I_{OUT}(mA)
E_{OUT}(V)
+125°C
25°C
-55°C
30Ω
50Ω
180
160
140
120
100
80
60
40
20
0.5
1.0
1.5
2.0
2.5
3.0
3.5V

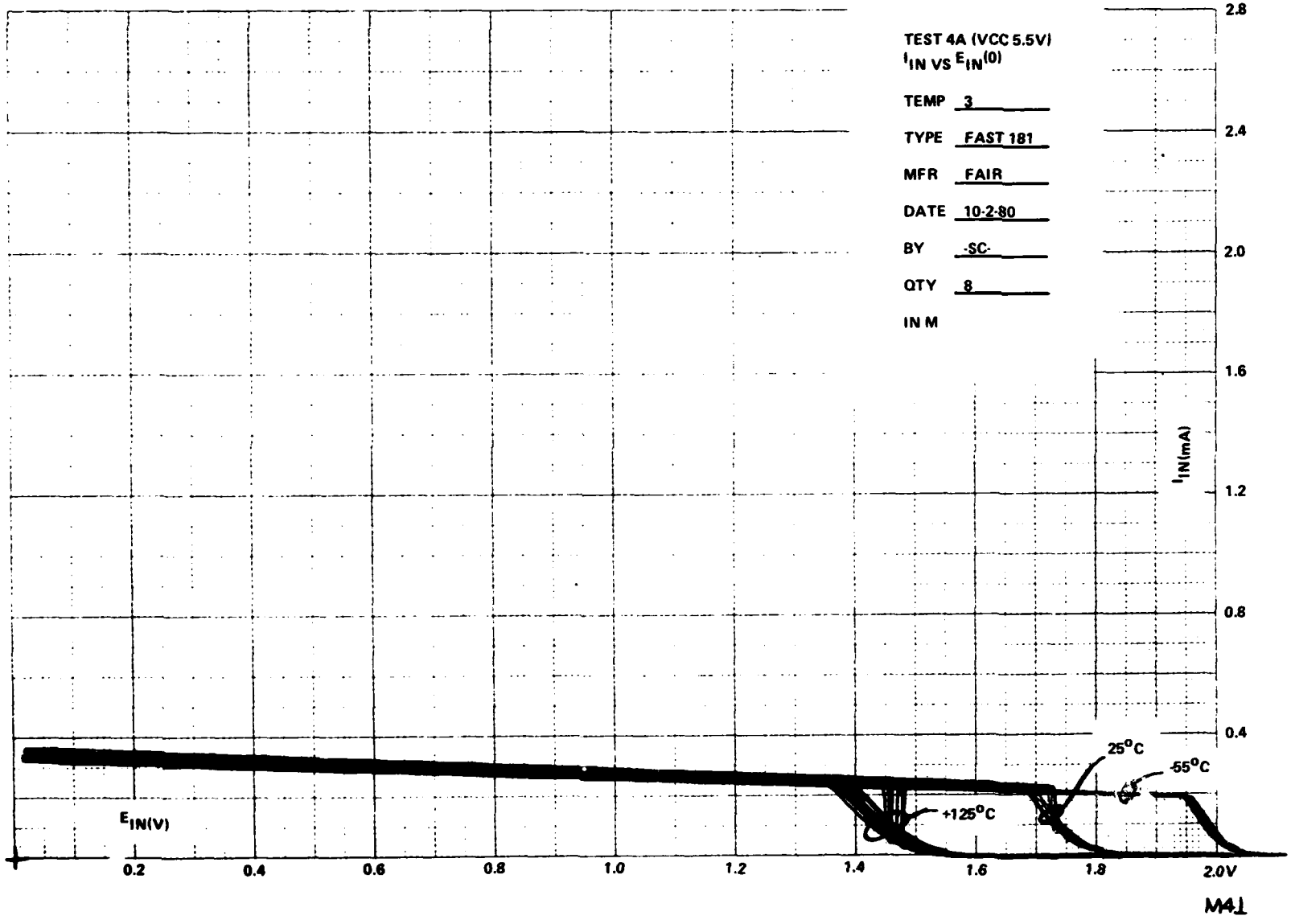

TEST 2 (VCC 5.5V)
IOUT VS EOUT(1)
TEMP 3
TYPE FAST 181
MFR FAIR
DATE 10-2-80
BY JC
QTY 8
S = SUM
A = 1 B = 0
B0 = 1 or 0
OUT F0, P, CN + 4
100 MA
90
80
70
60
50
40
30
20
10
IOUT(mA)
30Ω
50Ω
25°C
+125°C
-55°C
EOUT(V)
+
1
2
3
4
5
6
7V
M41

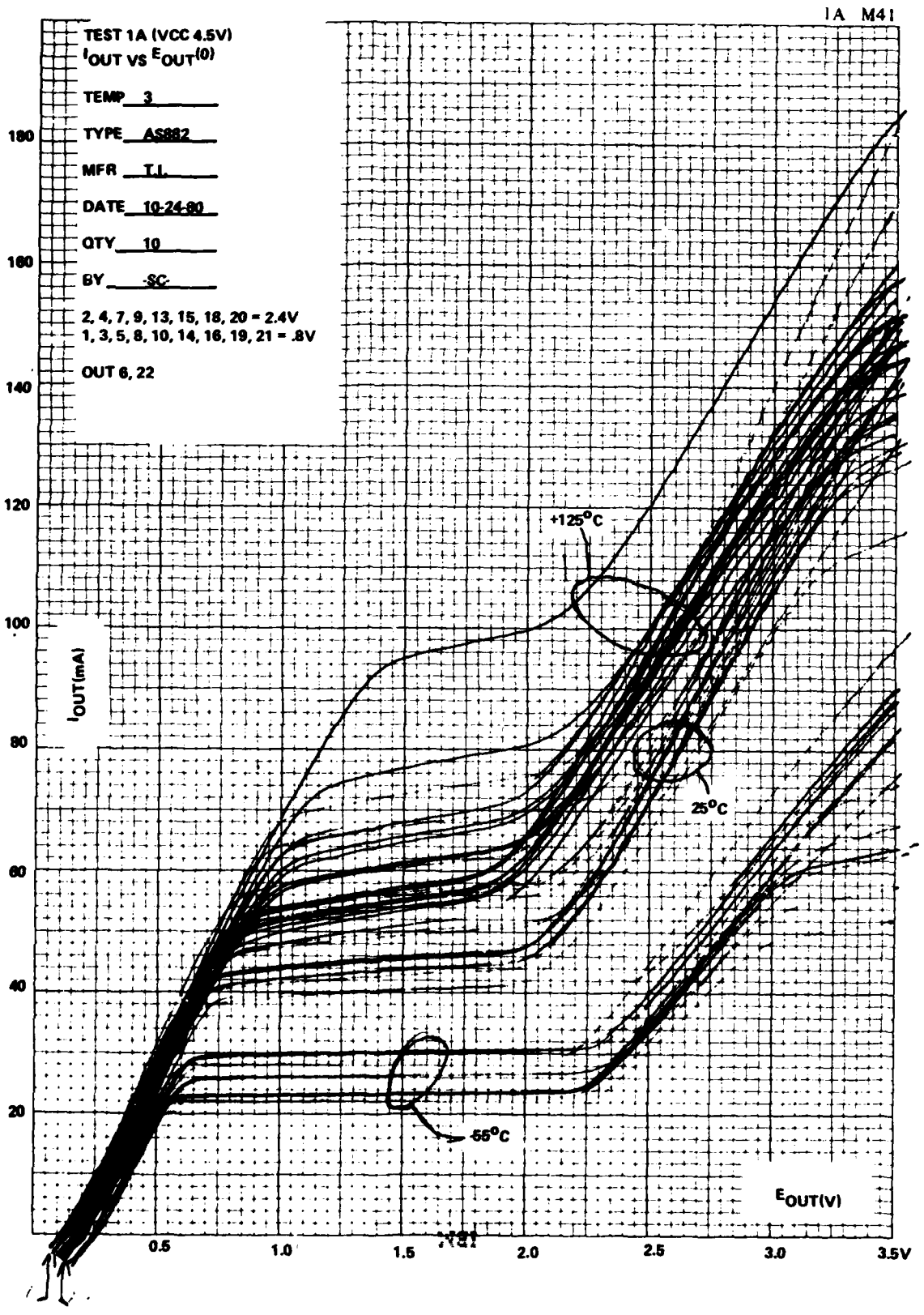

5 M41
TEST 5 (POWER)
I_{PS} VS E_{PS}
TEMP 3
TYPE FAST 181
MFG FAIR
DATE 10-2-80
QTY 8
BY JC
1, 2, 3, 6, 7, 19, 21, 23 = 2.4V
4, 5, 8, 18, 20, 22 = GND
90
80
70
60
50
40
30
20
10
$I_{PS(mA)}$
+125°C
25°C
-55°C
$E_{PS(V)}$
1
2
3
4
5
6
7V

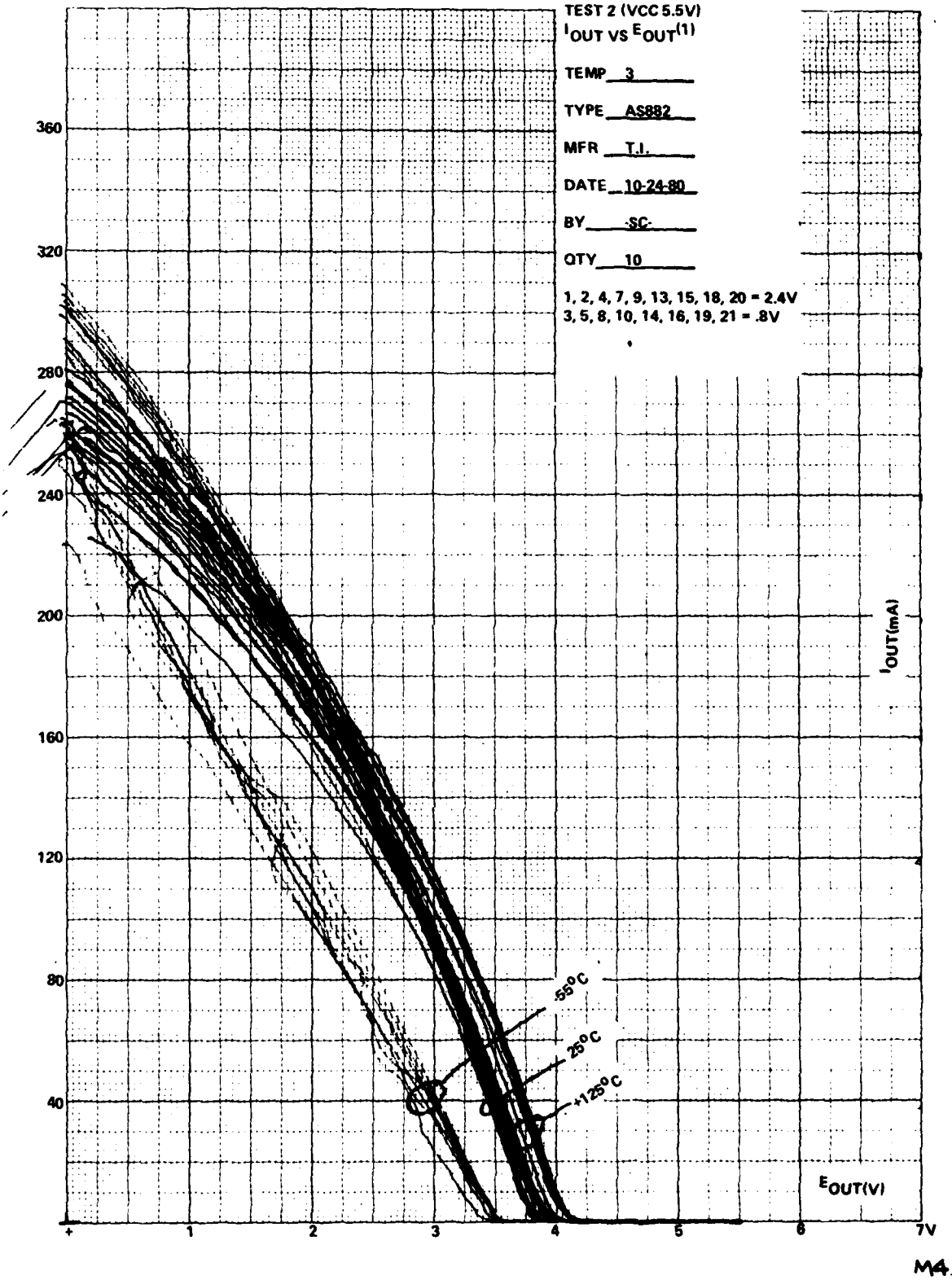

TEST 4A (VCC 5.5V)
I_{IN} VS $E_{IN}(0)$
TEMP 3
TYPE FAST 181
MFR FAIR
DATE 10-2-80
BY JC
QTY 8
IN A0
2.8
2.4
2.0
1.6
1.2
0.8
0.4
$I_{IN(mA)}$
+125°C
25°C
-55°C
$E_{IN(V)}$
.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
2.0V
M41


TEST 4A (VCC 5.5V)
I_{IN} VS $E_{IN}(0)$
TEMP 3
TYPE FAST 181
MFR FAIR
DATE 10-2-80
BY JC
QTY 8
IN B0
2.8
2.4
2.0
1.6
1.2
0.8
0.4
$I_{IN(mA)}$
+125°C
25°C
-55°C
$E_{IN(V)}$
.5
1
1.5
2.0
2.5
3.0
3.5
4.0
4.5

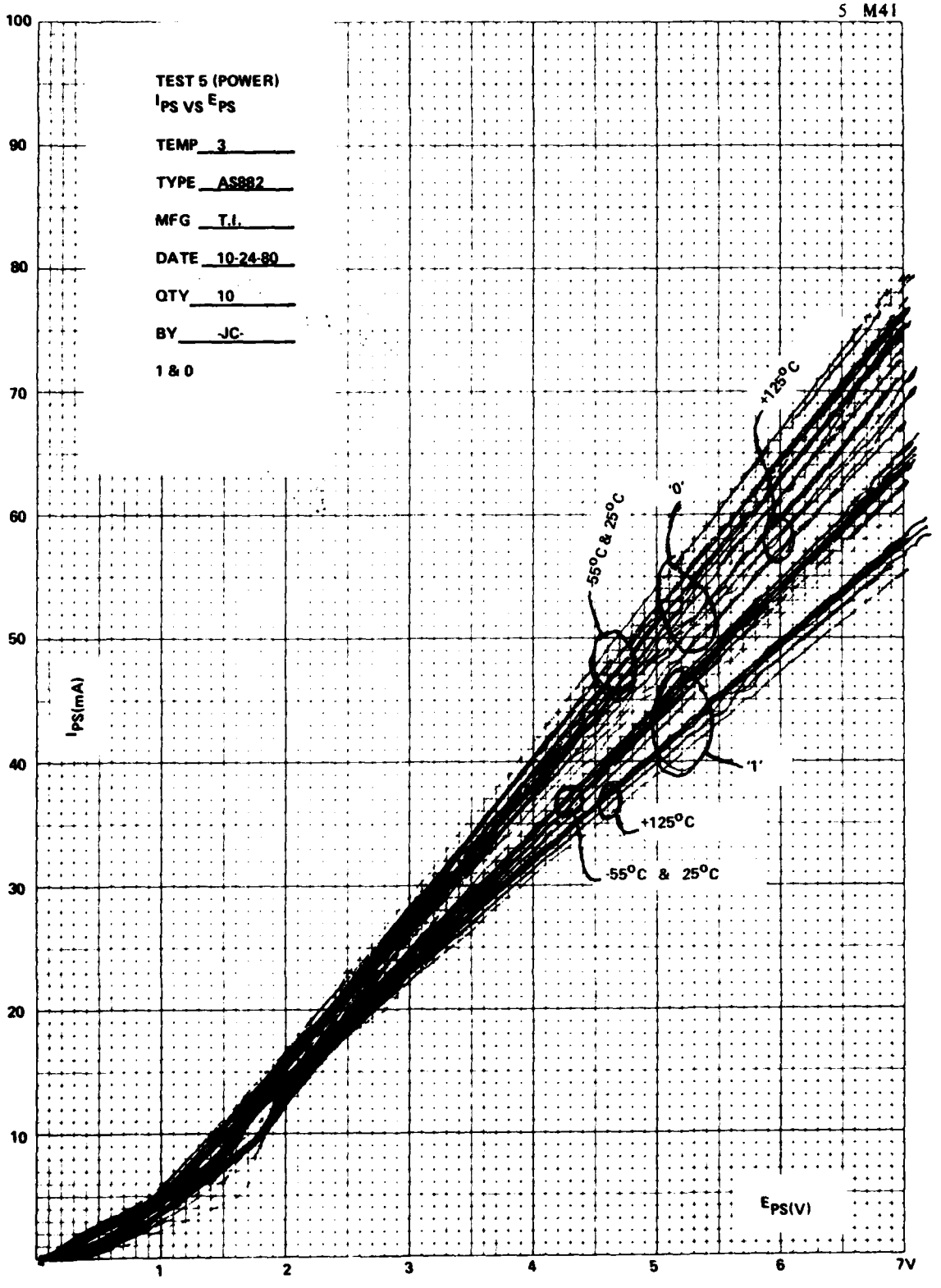

TEST 4A (VCC 5.5V)
I_{IN} VS E_{IN}(0)
TEMP 3
TYPE FAST 181
MFR FAIR
DATE 10-2-80
BY JC
QTY 8
IN CN
I_{IN}(mA)
E_{IN}(V)
-55°C
25°C
+125°C
MPAL

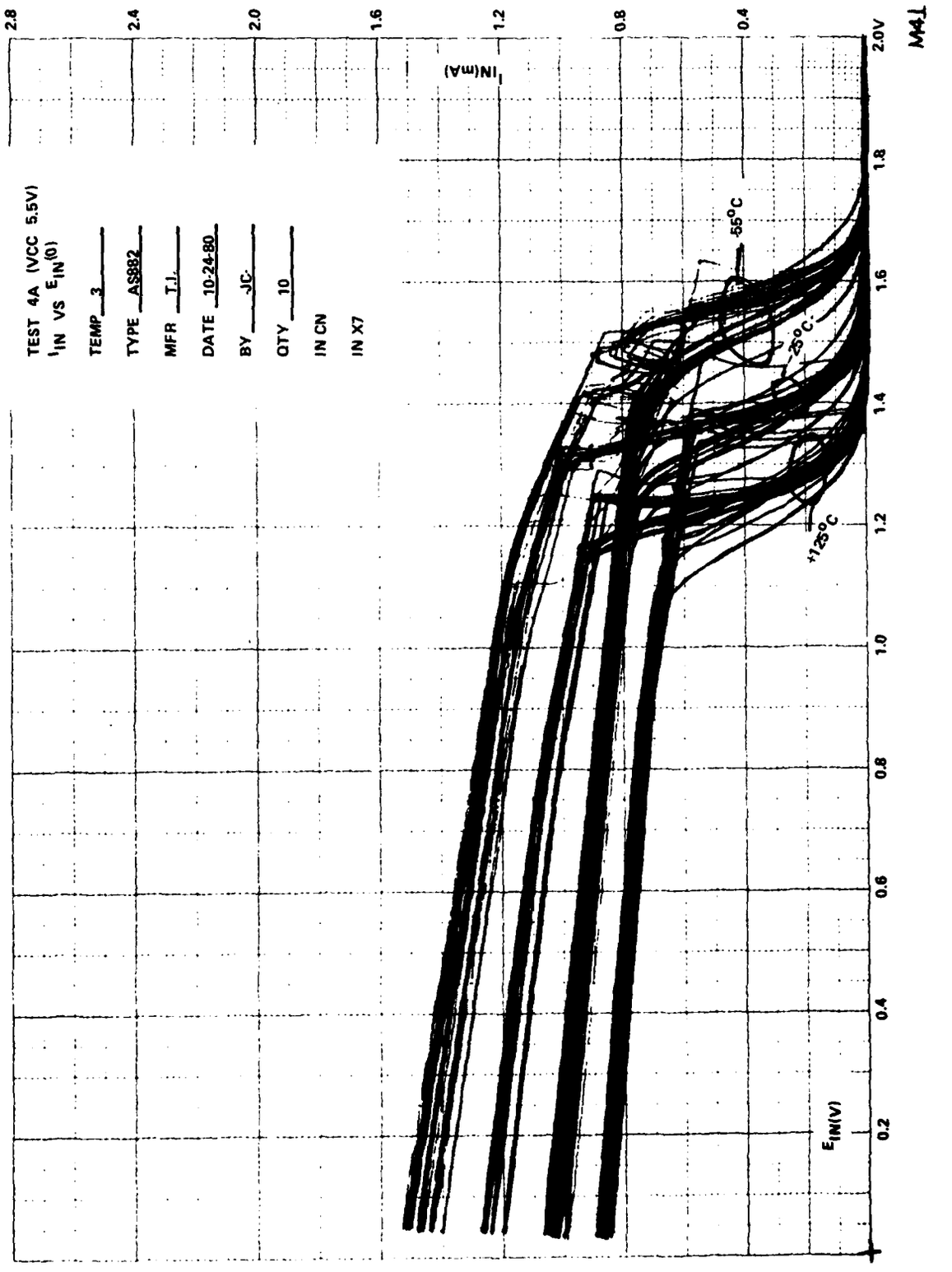

TEST 4A (VCC 5.5V)
I_{IN} VS $E_{IN}(0)$
TEMP 3
TYPE FAST 181
MFR FAIR
DATE 10-2-80
BY -SC-
QTY 8
IN M
2.8
2.4
2.0
1.6
1.2
0.8
0.4
I_{IN}(mA)
25°C
-55°C
+125°C
$E_{IN(V)}$
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0V
M41

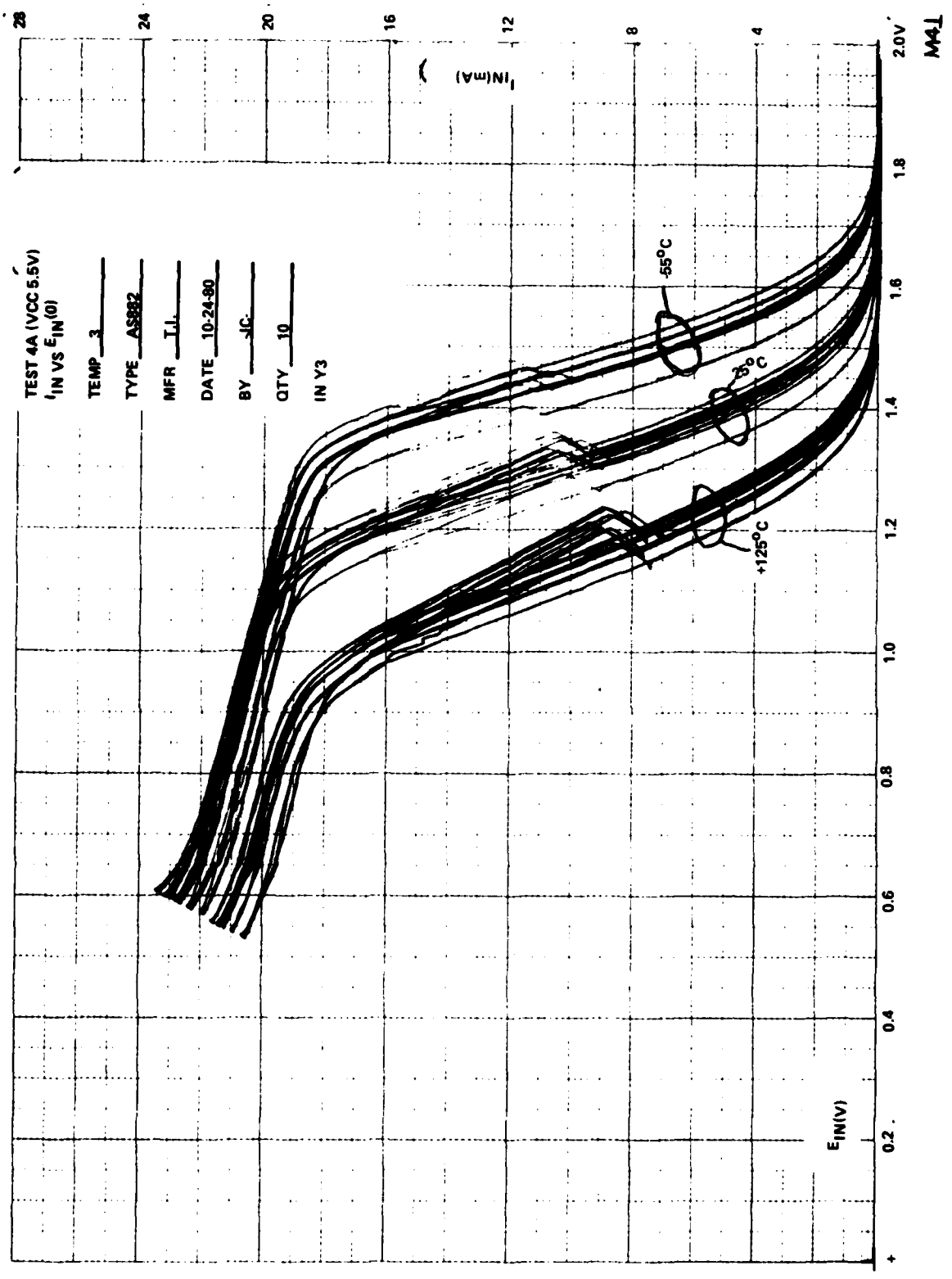

1A M41
TEST 1A (VCC 4.5V)
I_{OUT} VS E_{OUT}(0)
TEMP 3
TYPE AS882
MFR T.I.
DATE 10-24-80
QTY 10
BY SC
2, 4, 7, 9, 13, 15, 18, 20 = 2.4V
1, 3, 5, 8, 10, 14, 16, 19, 21 = .8V
OUT 6, 22
+125°C
25°C
-55°C
I_{OUT}(mA)
E_{OUT}(V)
180
160
140
120
100
80
60
40
20
0.5
1.0
1.5
2.0
2.5
3.0
3.5V

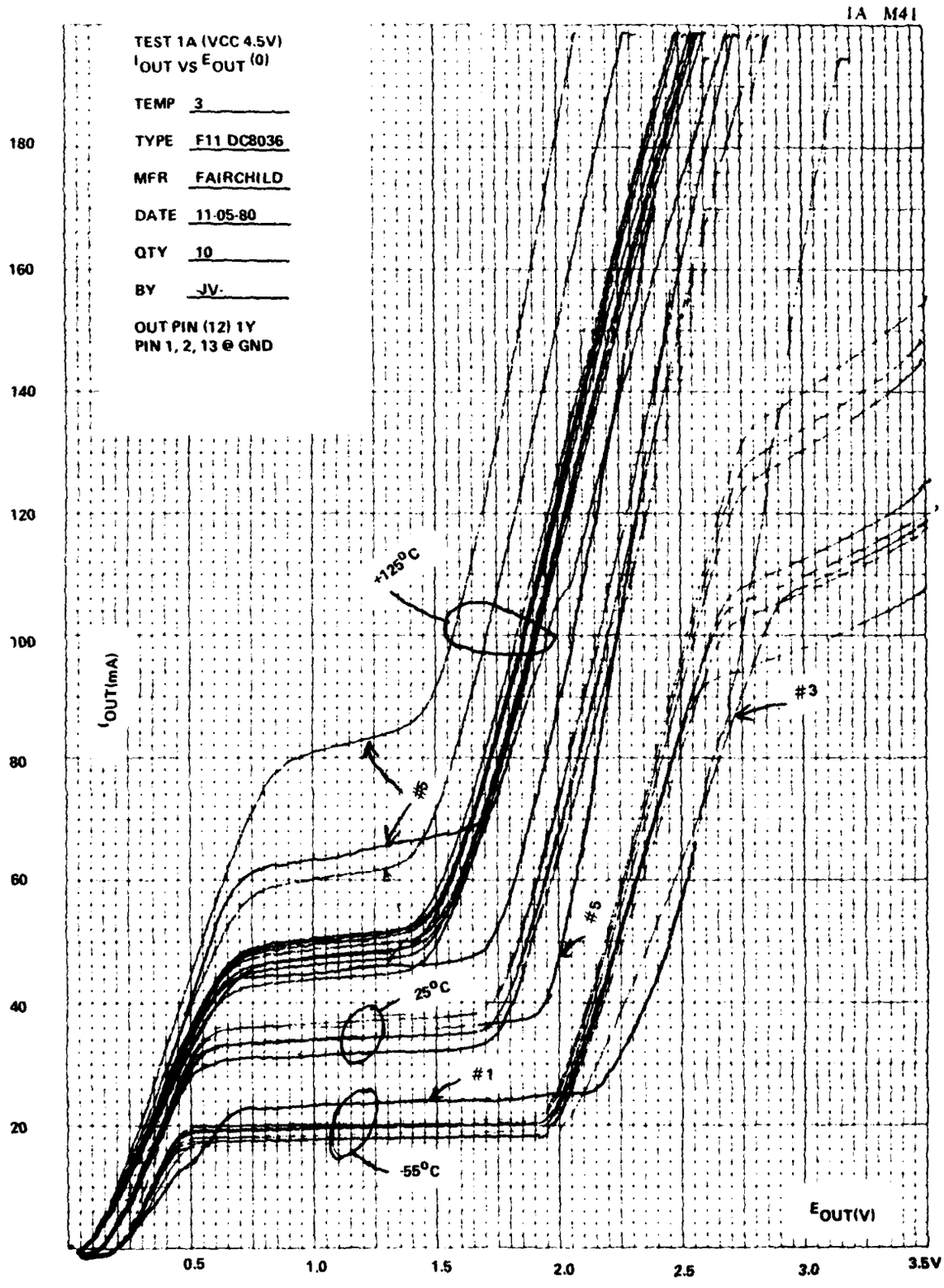

TEST 2 (VCC 5.5V)
I_{OUT} VS E_{OUT}(1)
TEMP 3
TYPE AS882
MFR T.I.
DATE 10-24-80
BY SC
QTY 10
1, 2, 4, 7, 9, 13, 15, 18, 20 = 2.4V
3, 5, 8, 10, 14, 16, 19, 21 = .8V
360
320
280
240
200
160
120
80
40
I_{OUT}(mA)
-55°C
25°C
+125°C
E_{OUT}(V)
+
1
2
3
4
5
6
7V

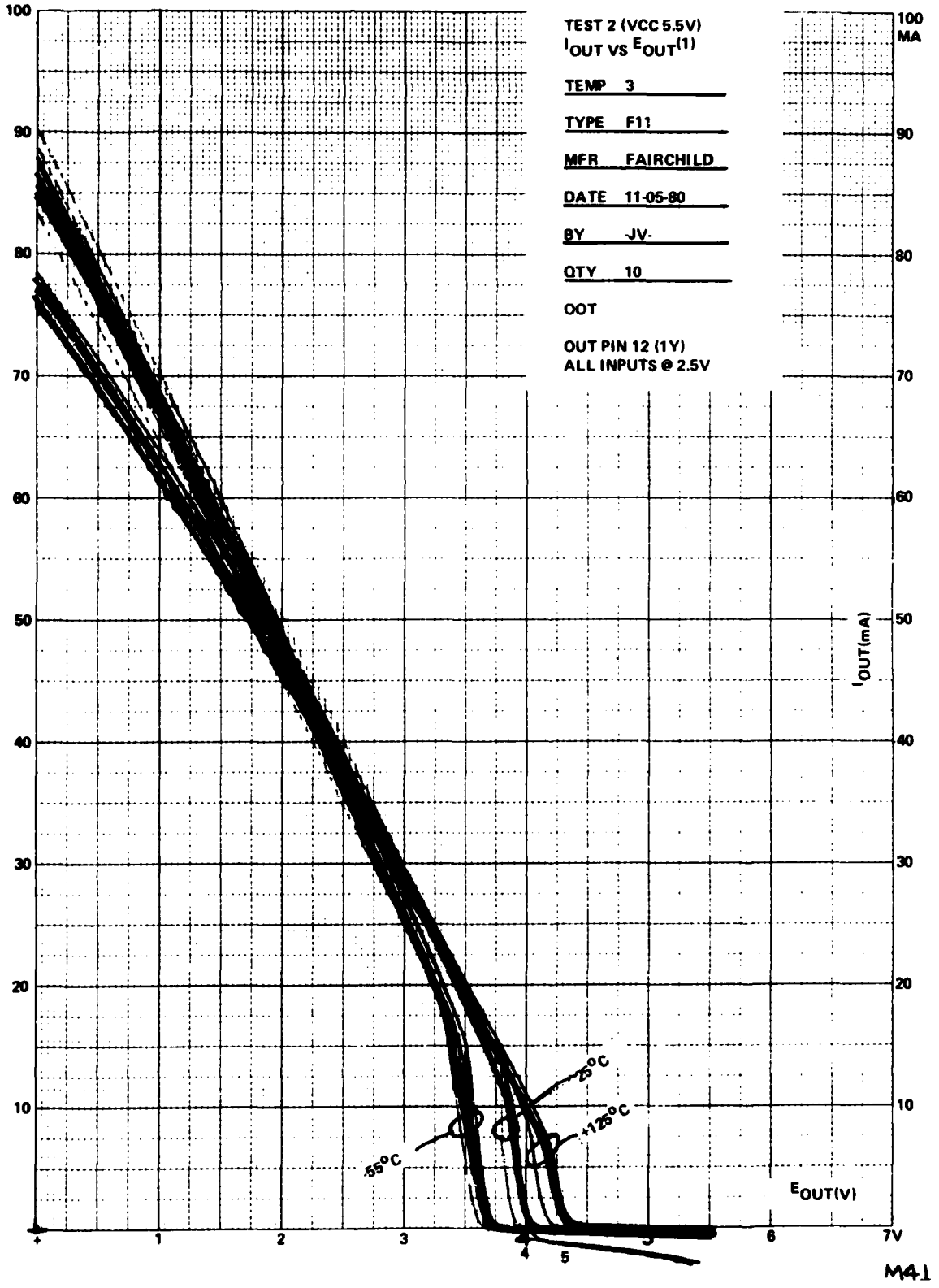
M41

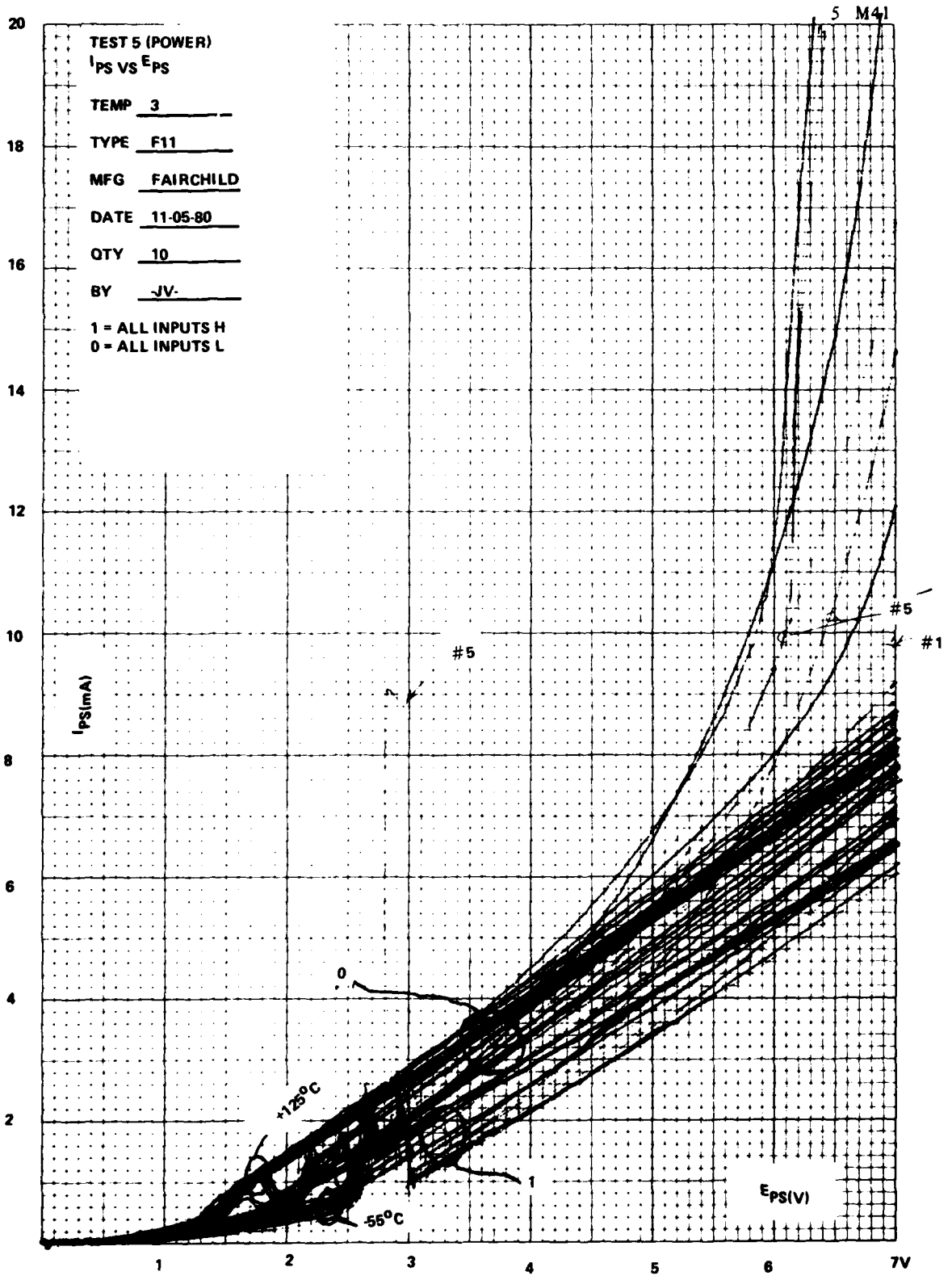

TEST 5 (POWER)
I_{PS} VS E_{PS}
TEMP 3
TYPE AS882
MFG T.I.
DATE 10-24-80
QTY 10
BY JC
1 & 0
$I_{PS(mA)}$
$E_{PS(V)}$
100
90
80
70
60
50
40
30
20
10
1
2
3
4
5
6
7V
+125°C
'0'
-55°C & 25°C
'1'
+125°C
-55°C & 25°C

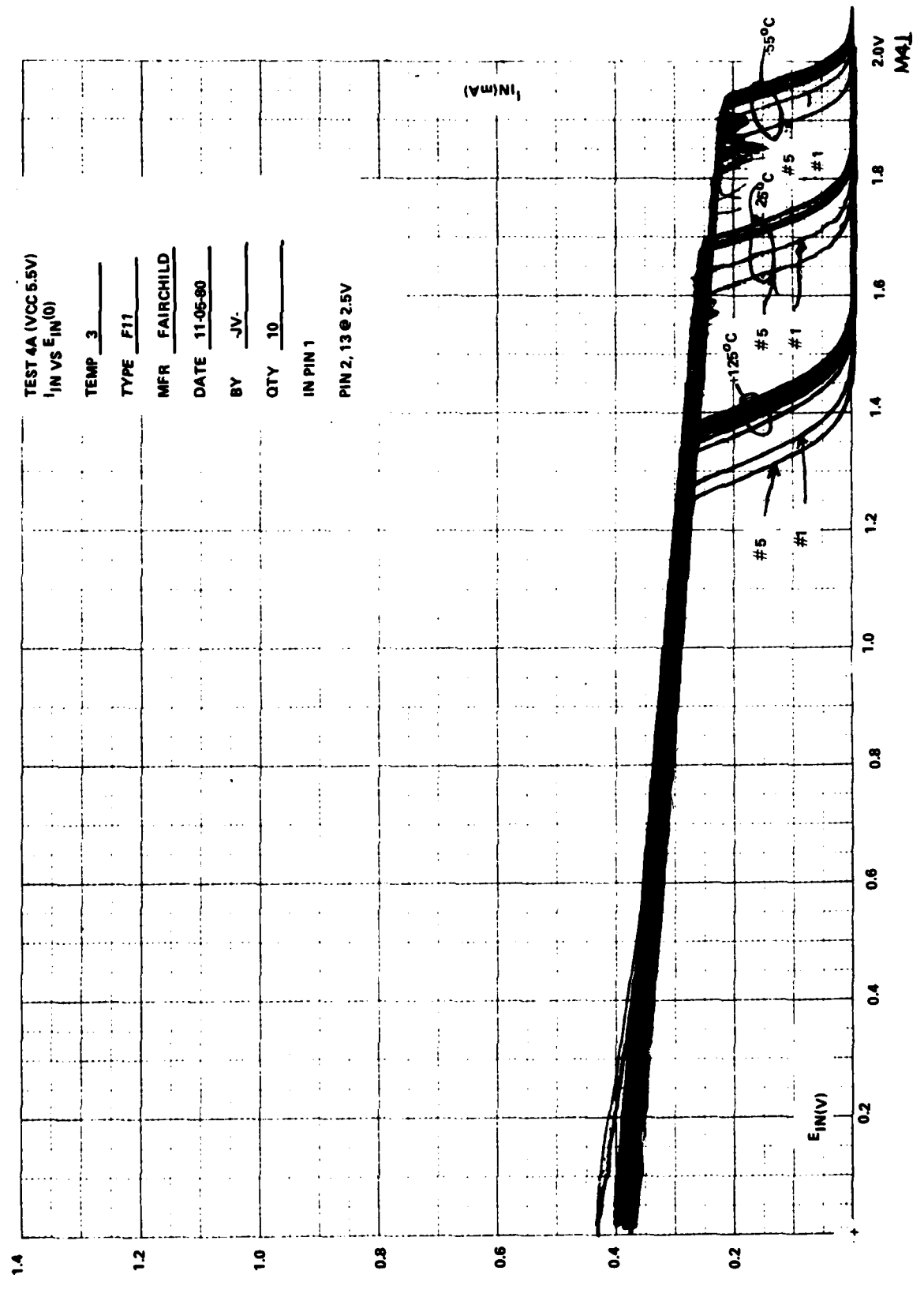

TEST 4A (VCC 5.5V)
I_{IN} VS $E_{IN}(0)$
TEMP 3
TYPE AS882
MFR T.I.
DATE 10-24-80
BY JC
QTY 10
IN CN
IN X7
I_{IN}(mA)
E_{IN}(V)
-55°C
25°C
+125°C
M41

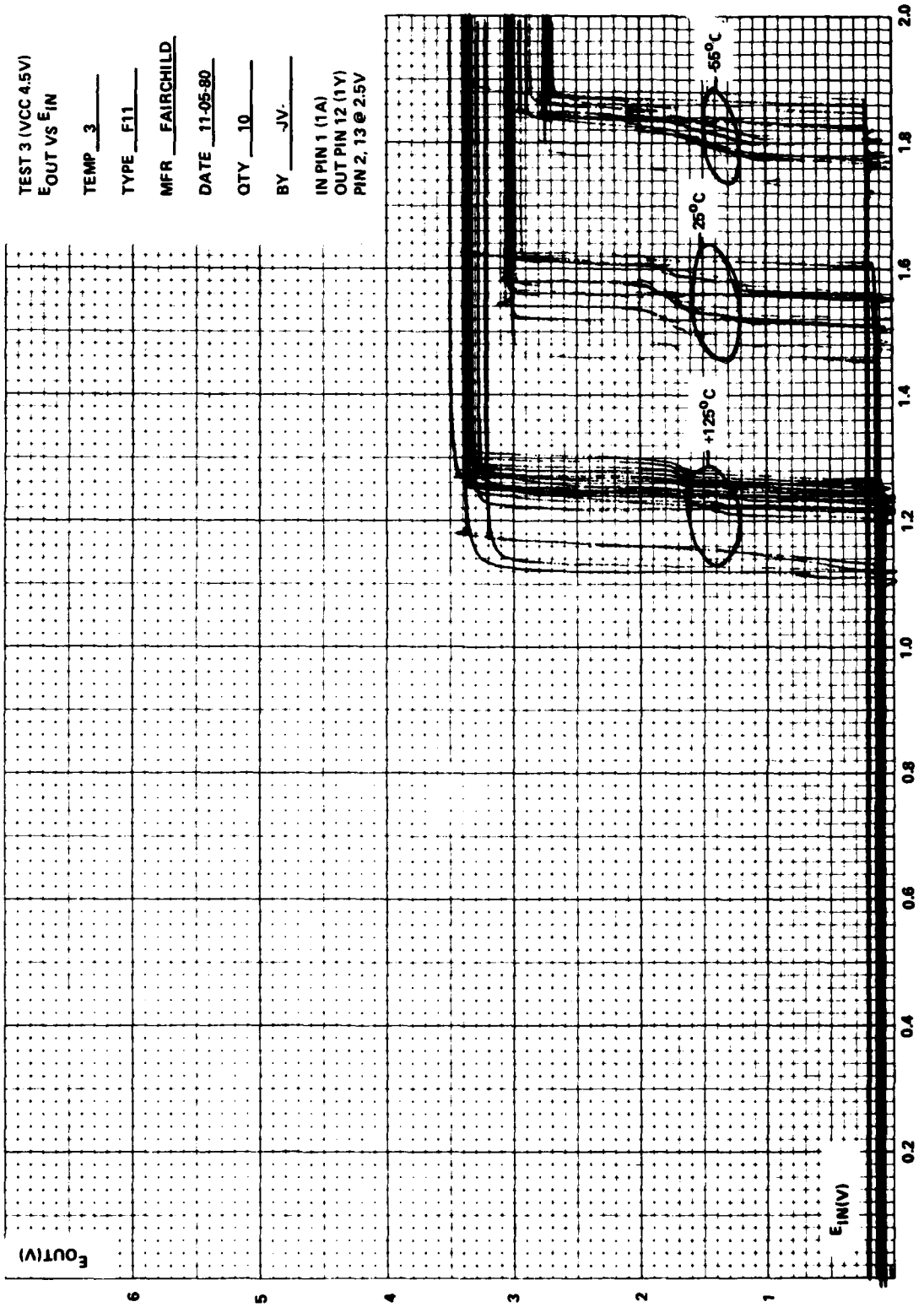

TEST 4A (VCC 5.5V)
I_{IN} VS E_{IN}(0)
TEMP 3
TYPE AS882
MFR T.I.
DATE 10-24-80
BY JC
QTY 10
IN Y3
-55°C
25°C
+125°C
I_{IN}(mA)
E_{IN}(V)
28
24
20
16
12
8
4
+
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0V
TYP

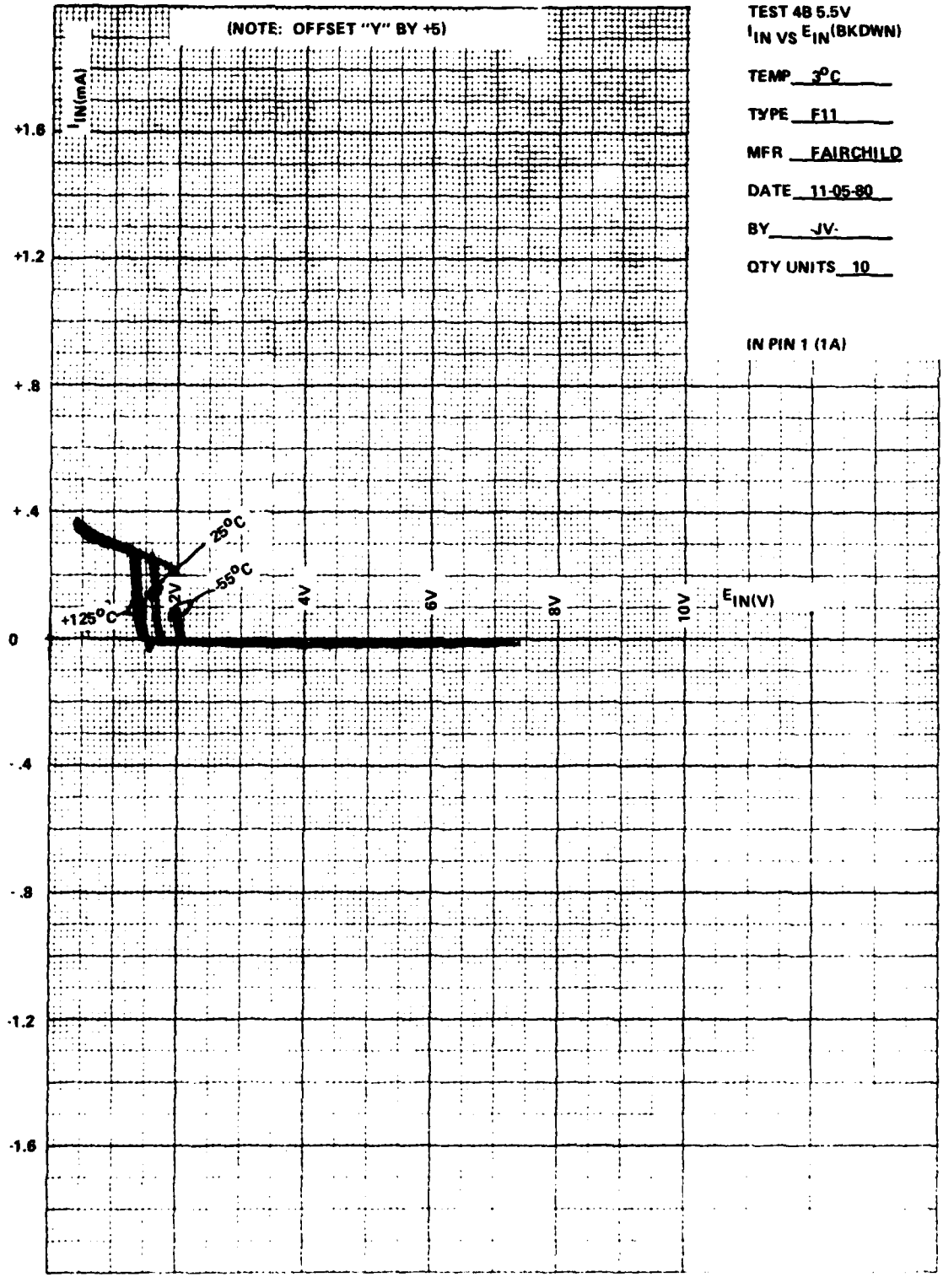

1A M41
TEST 1A (VCC 4.5V)
I_{OUT} VS E_{OUT} (0)
TEMP 3
TYPE F11 DC8036
MFR FAIRCHILD
DATE 11-05-80
QTY 10
BY JV
OUT PIN (12) 1Y
PIN 1, 2, 13 @ GND
180
160
140
120
100
80
60
40
20
I_{OUT}(mA)
+125°C
#3
#4
#5
25°C
#1
-55°C
0.5
1.0
1.5
2.0
2.5
3.0
3.5V
E_{OUT}(V)

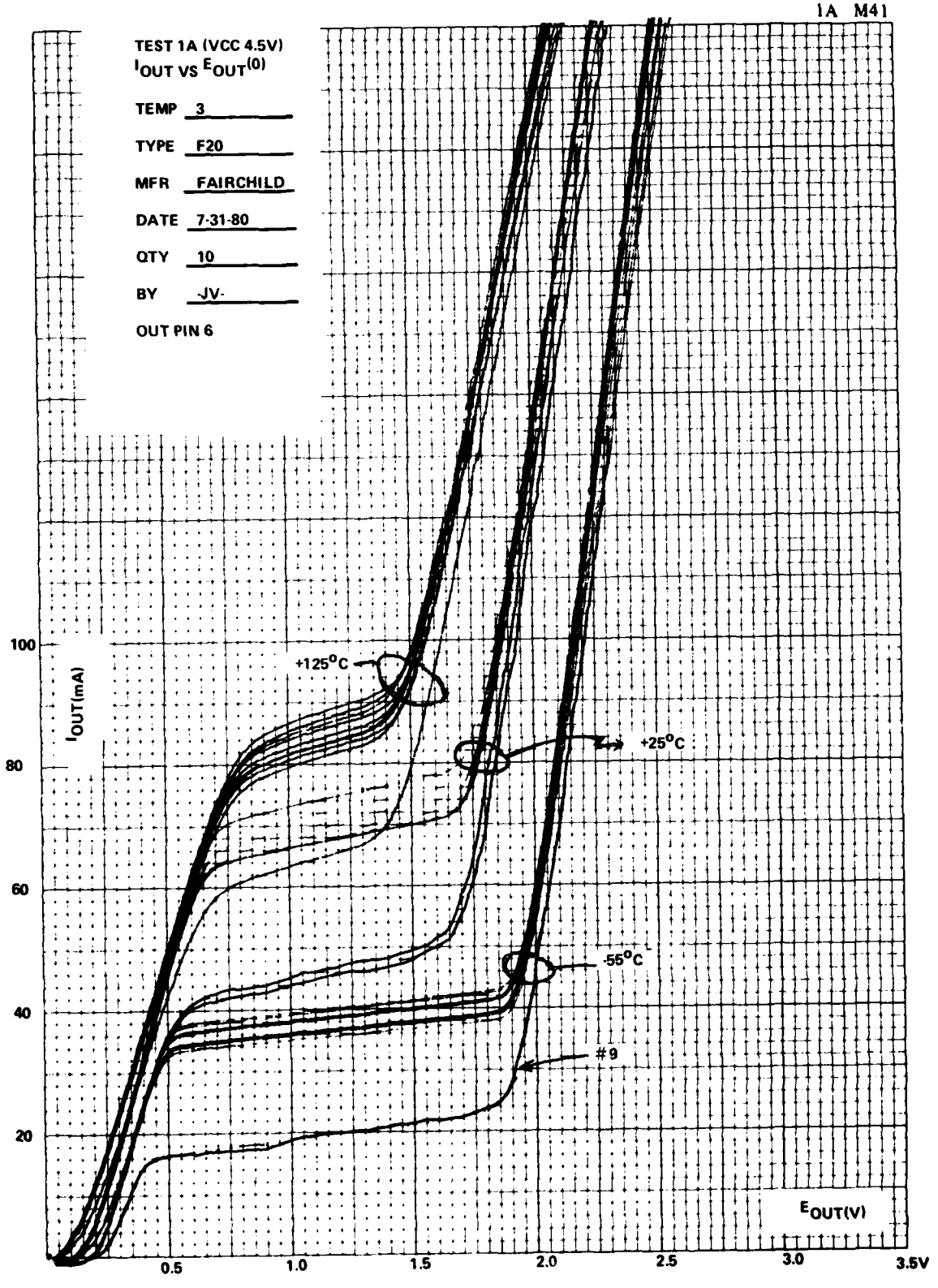

TEST 2 (VCC 5.5V)
I_{OUT} VS E_{OUT}(1)
TEMP 3
TYPE F11
MFR FAIRCHILD
DATE 11-05-80
BY -JV-
QTY 10
OOT
OUT PIN 12 (1Y)
ALL INPUTS @ 2.5V
100 MA
90
80
70
60
50
40
30
20
10
I_{OUT}(mA)
+125°C
25°C
-55°C
E_{OUT}(V)
1
2
3
4
5
6
7V
M41

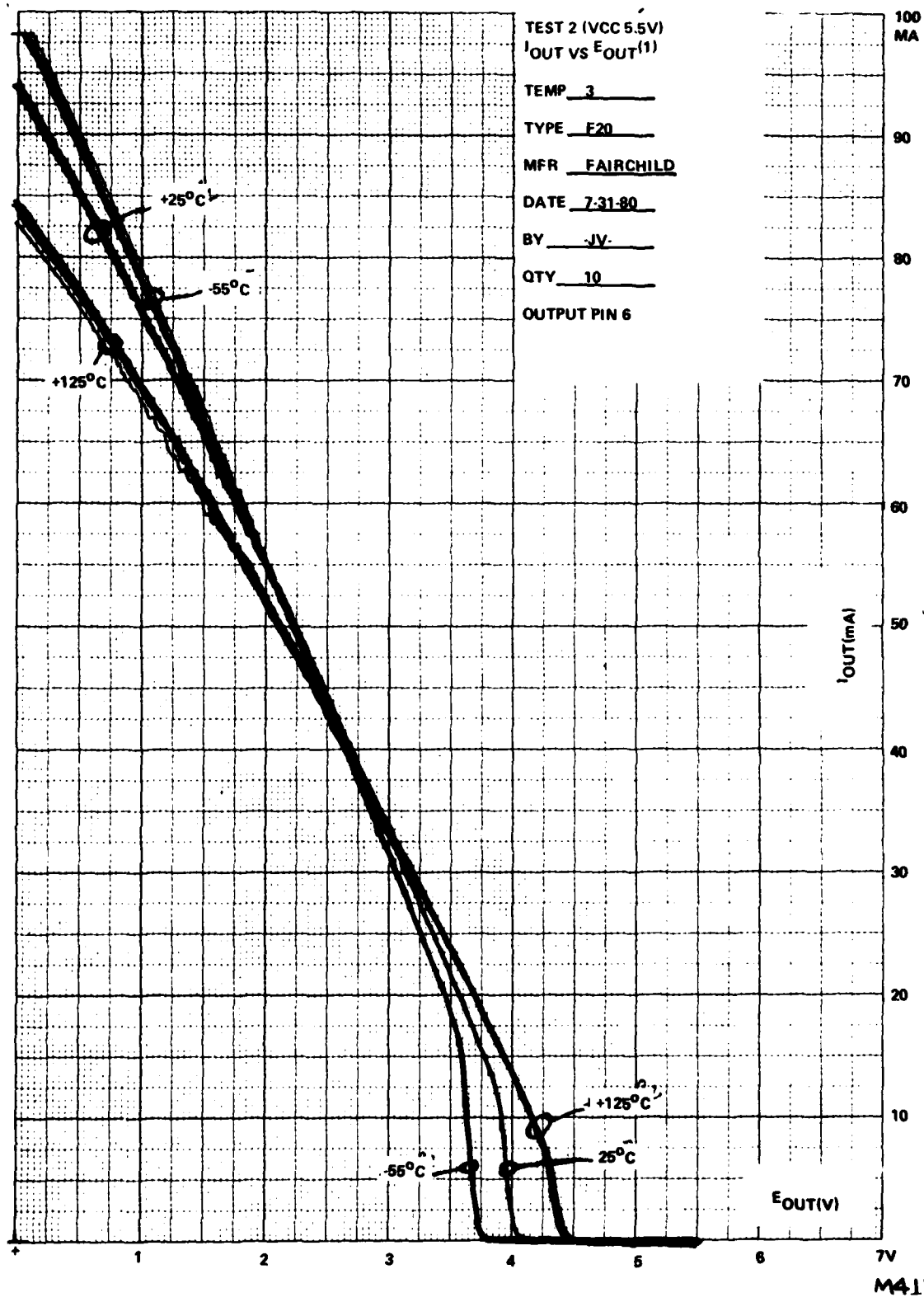

5 M41
TEST 5 (POWER)
I_{PS} VS E_{PS}
TEMP 3
TYPE F11
MFG FAIRCHILD
DATE 11-05-80
QTY 10
BY -JV-
1 = ALL INPUTS H
0 = ALL INPUTS L
20
18
16
14
12
10
8
6
4
2
$I_{PS(mA)}$
#5
#5
#1
0
+125°C
-55°C
1
$E_{PS(V)}$
1
2
3
4
5
6
7V

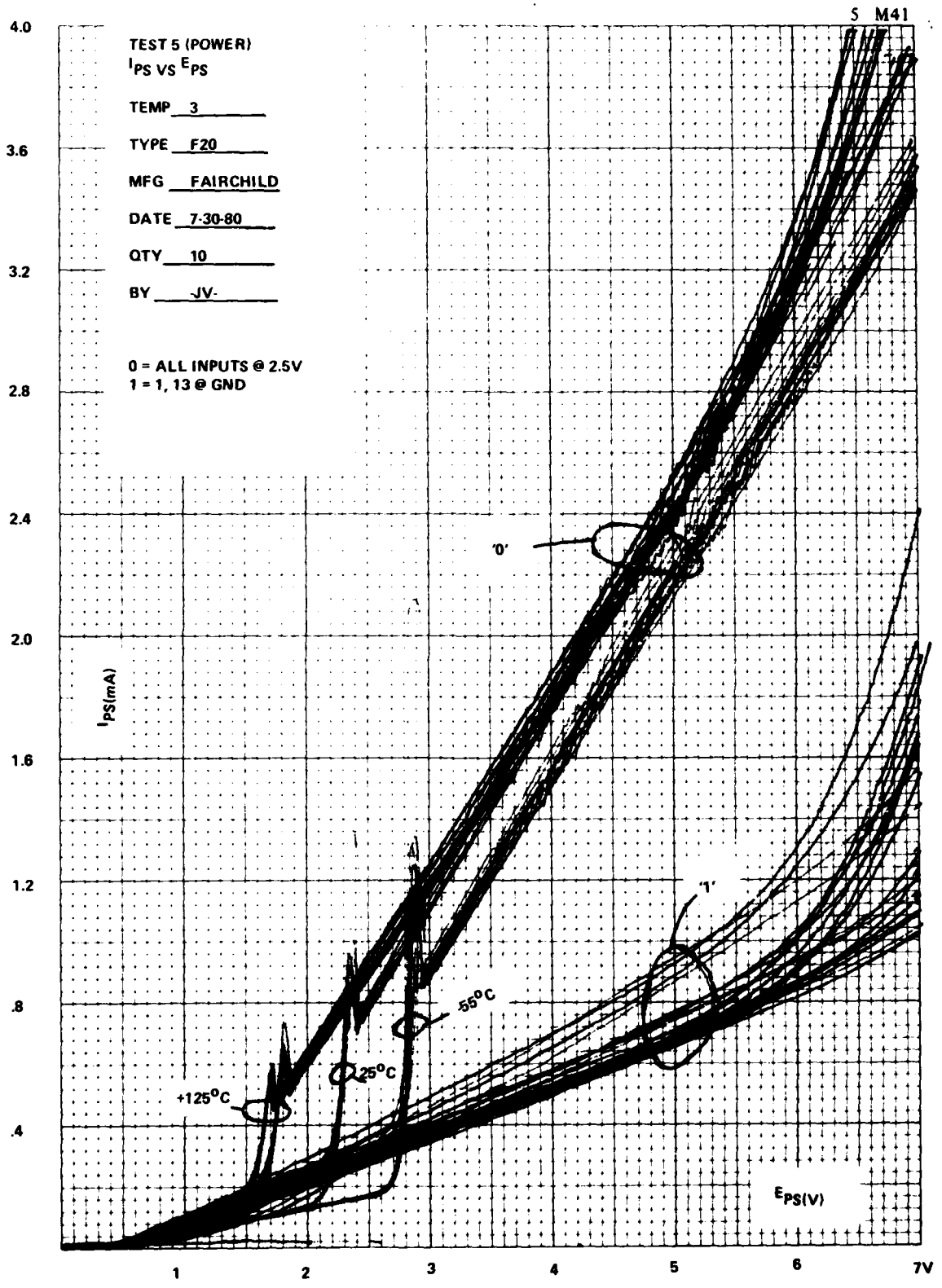

TEST 4A (VCC 5.5V)
I_{IN} VS E_{IN}(0)
TEMP 3
TYPE F11
MFR FAIRCHILD
DATE 11-05-80
BY JV
QTY 10
IN PIN 1
PIN 2, 13 @ 2.5V
I_{IN}(mA)
E_{IN}(V)
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0V
-55°C
25°C
125°C
#5
#1
TM41

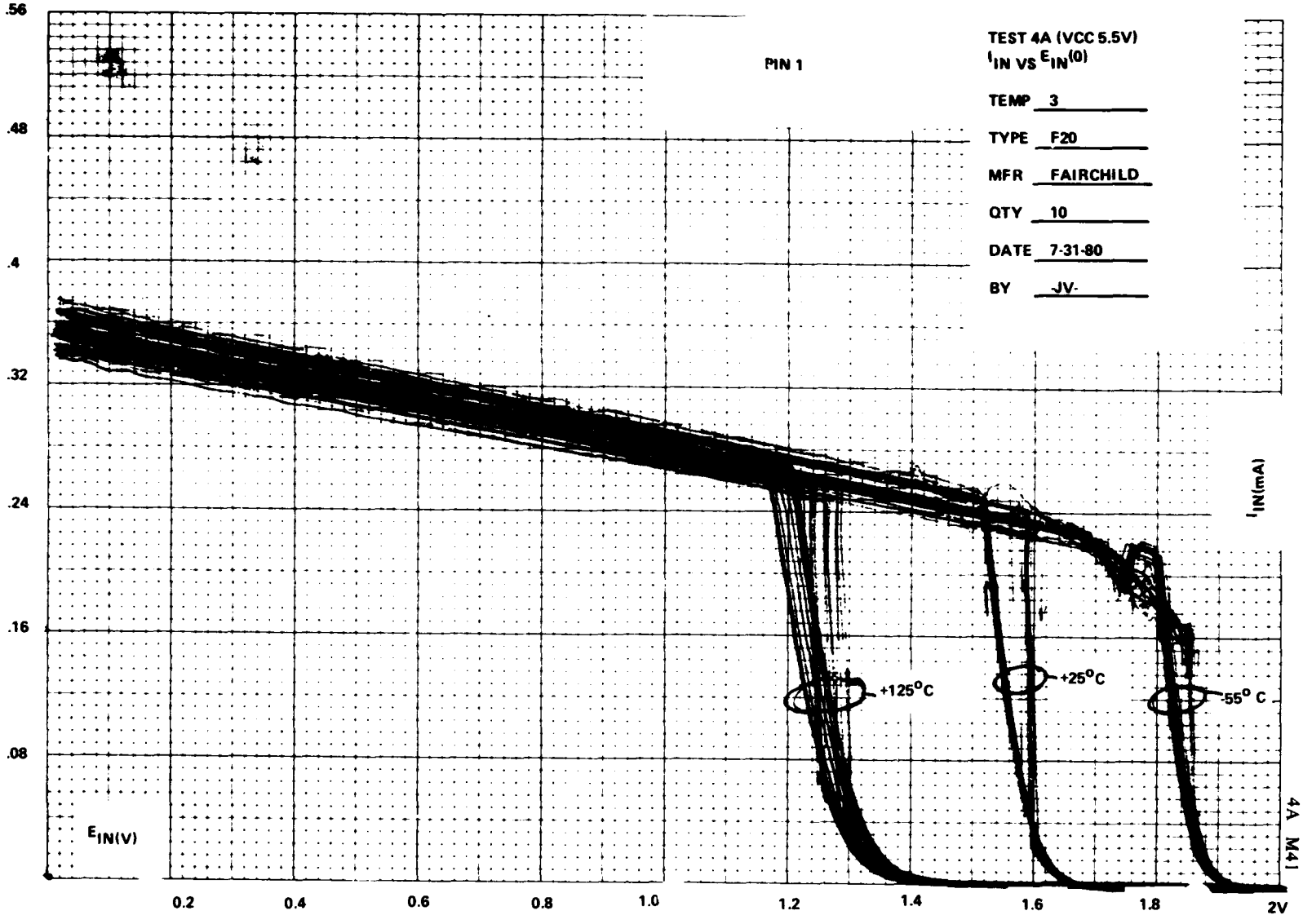

TEST 3 (VCC 4.5V)
E_{OUT} VS E_{IN}
TEMP 3
TYPE F11
MFR FAIRCHILD
DATE 11-05-80
QTY 10
BY JV
IN PIN 1 (1A)
OUT PIN 12 (1Y)
PIN 2, 13 @ 2.5V
E_{OUT}(V)
E_{IN}(V)
+125°C
25°C
-55°C
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
1
2
3
4
5
6

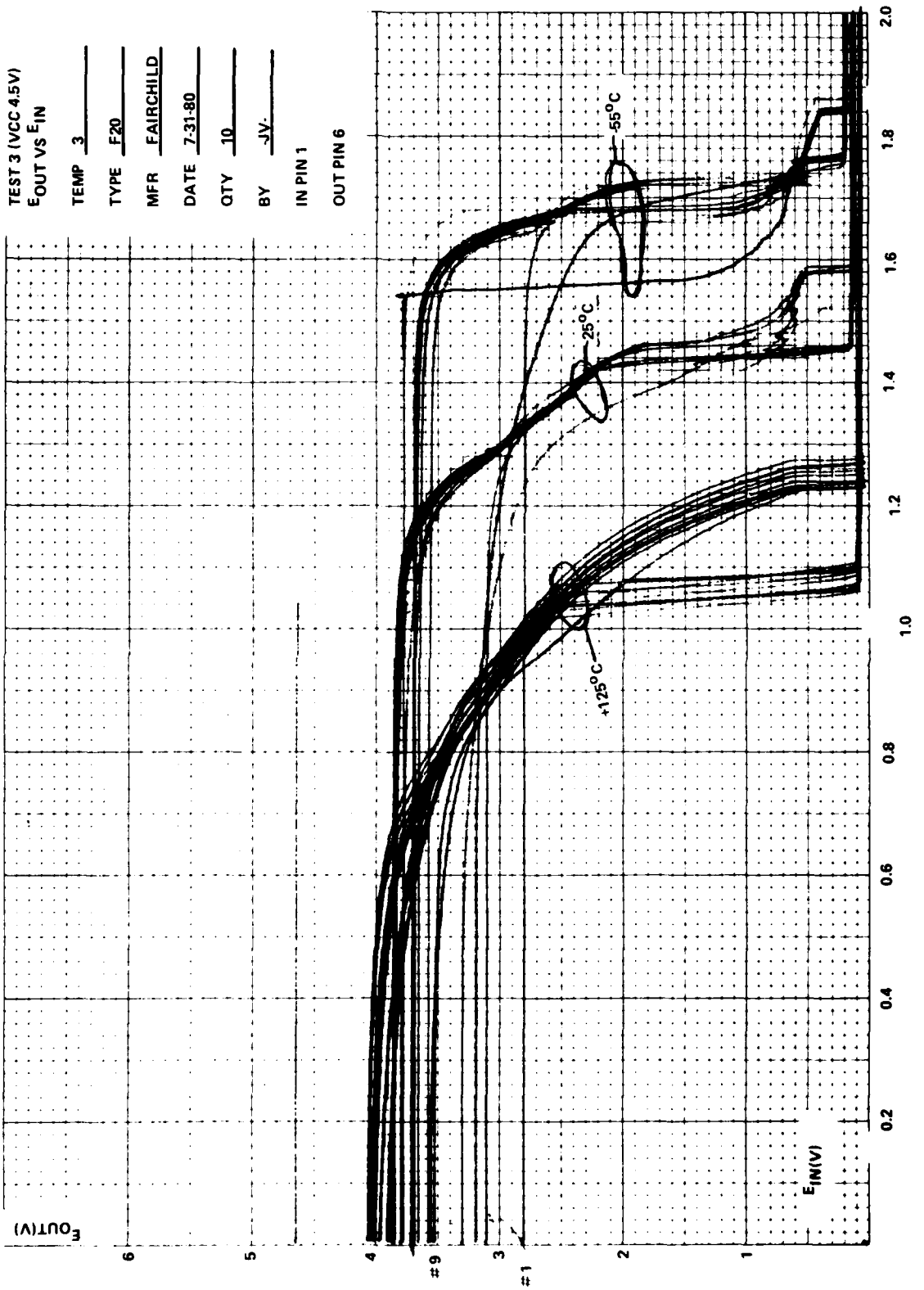

(NOTE: OFFSET "Y" BY +5)
TEST 48 5.5V
I_{IN} VS E_{IN}(BKDWN)
TEMP 3°C
TYPE F11
MFR FAIRCHILD
DATE 11-05-80
BY JV
QTY UNITS 10
(N PIN 1 (1A)
I_{IN}(mA)
+1.6
+1.2
+ .8
+ .4
0
- .4
- .8
-1.2
-1.6
25°C
-55°C
+125°C
2V
4V
6V
8V
10V
E_{IN}(V)

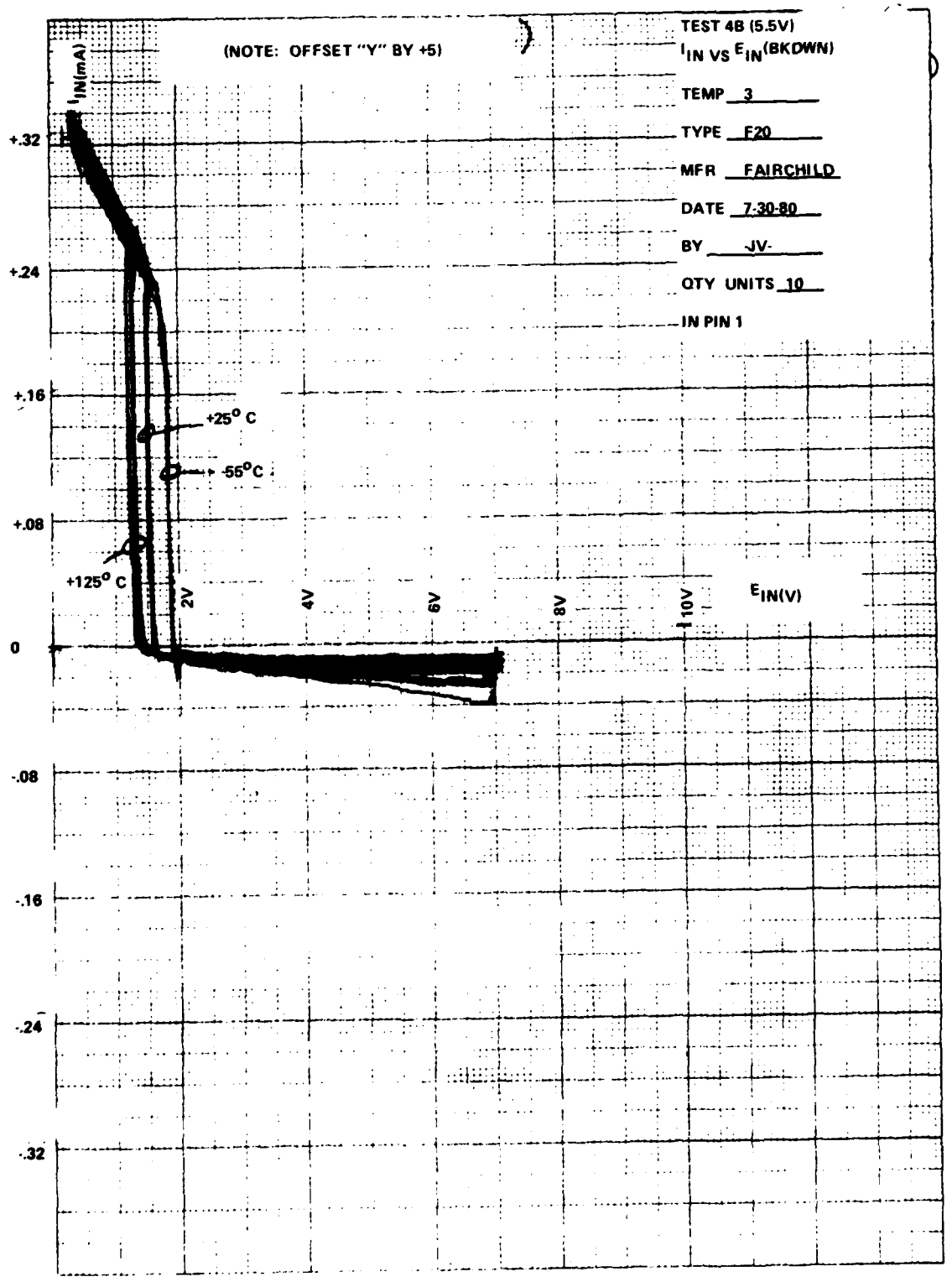

1A M41
TEST 1A (VCC 4.5V)
I_{OUT} VS E_{OUT}(0)
TEMP 3
TYPE F20
MFR FAIRCHILD
DATE 7-31-80
QTY 10
BY -JV-
OUT PIN 6
100
80
60
40
20
I_{OUT}(mA)
+125°C
+25°C
-55°C
#9
0.5
1.0
1.5
2.0
2.5
3.0
3.5V
E_{OUT}(V)

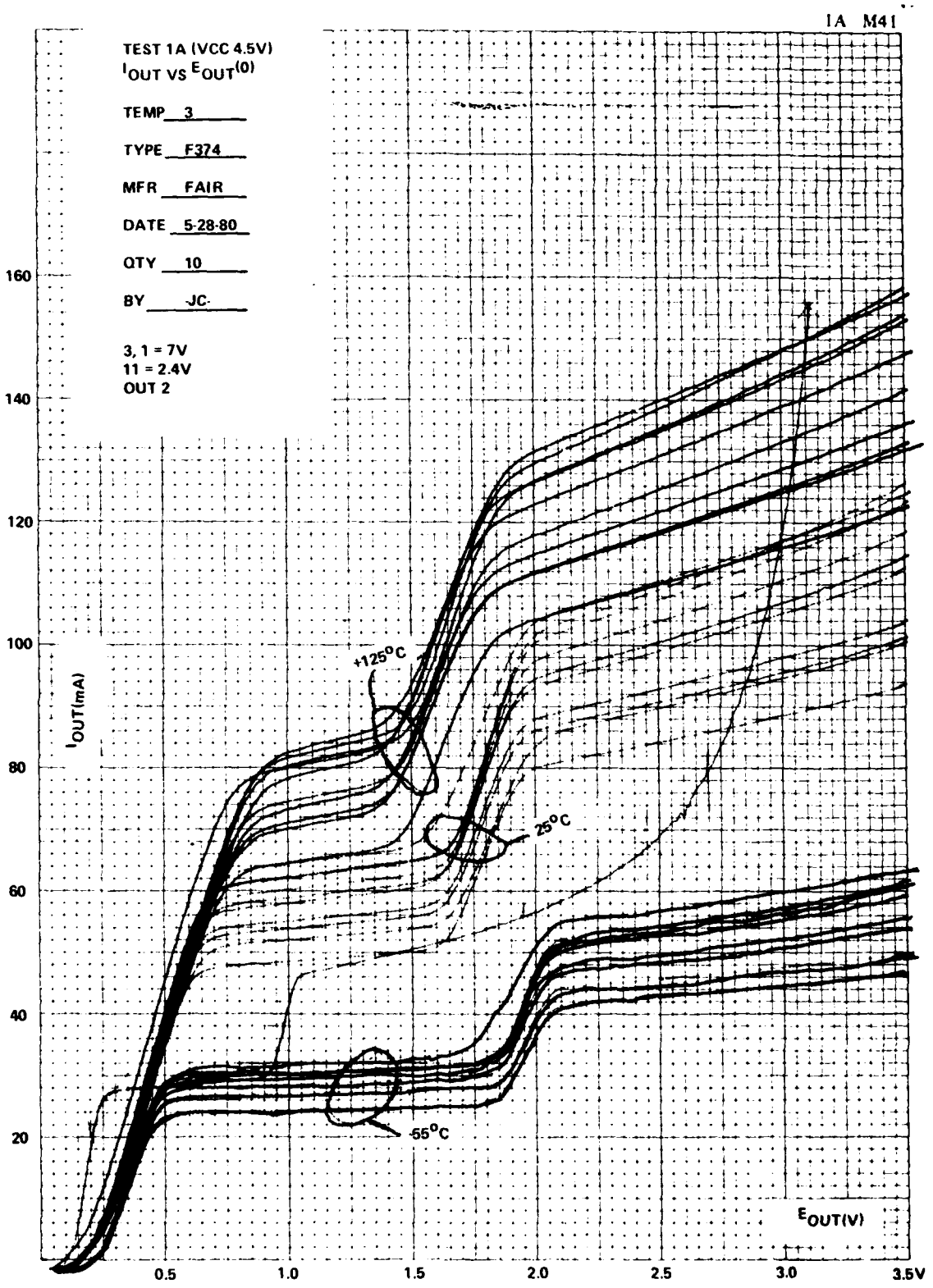

TEST 2 (VCC 5.5V)
I_{OUT} VS E_{OUT}(1)
TEMP 3
TYPE F20
MFR FAIRCHILD
DATE 7-31-80
BY JV
QTY 10
OUTPUT PIN 6
+25°C
-55°C
+125°C
+125°C
25°C
-55°C
100 MA
90
80
70
60
50
40
30
20
10
I_{OUT}(mA)
E_{OUT}(V)
+
1
2
3
4
5
6
7V
M41

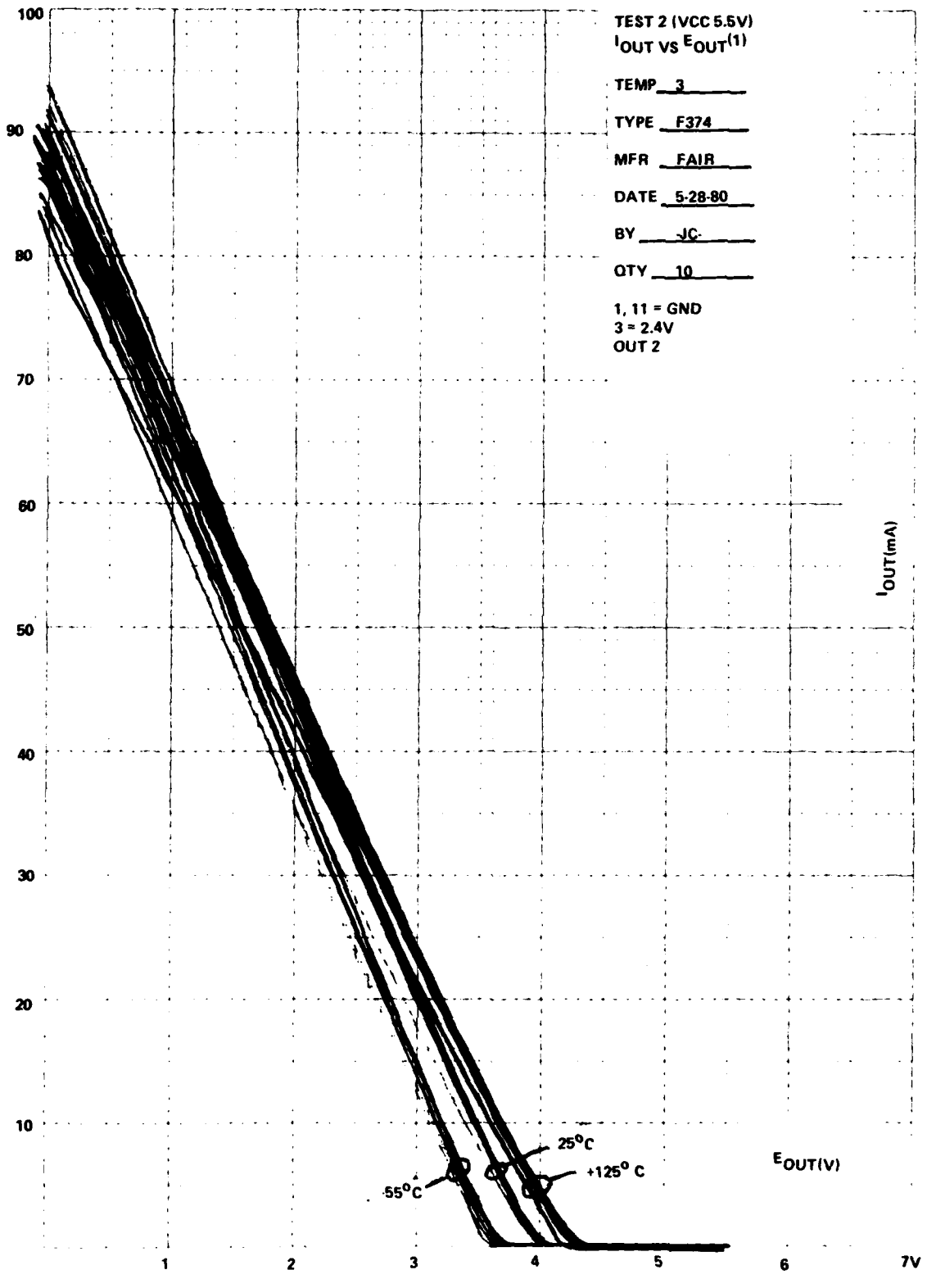

5 M41
TEST 5 (POWER)
I_{PS} VS E_{PS}
TEMP 3
TYPE F20
MFG FAIRCHILD
DATE 7-30-80
QTY 10
BY -JV-
0 = ALL INPUTS @ 2.5V
1 = 1, 13 @ GND
4.0
3.6
3.2
2.8
2.4
2.0
1.6
1.2
.8
.4
$I_{PS(mA)}$
'0'
'1'
55°C
25°C
+125°C
$E_{PS(V)}$
1
2
3
4
5
6
7V

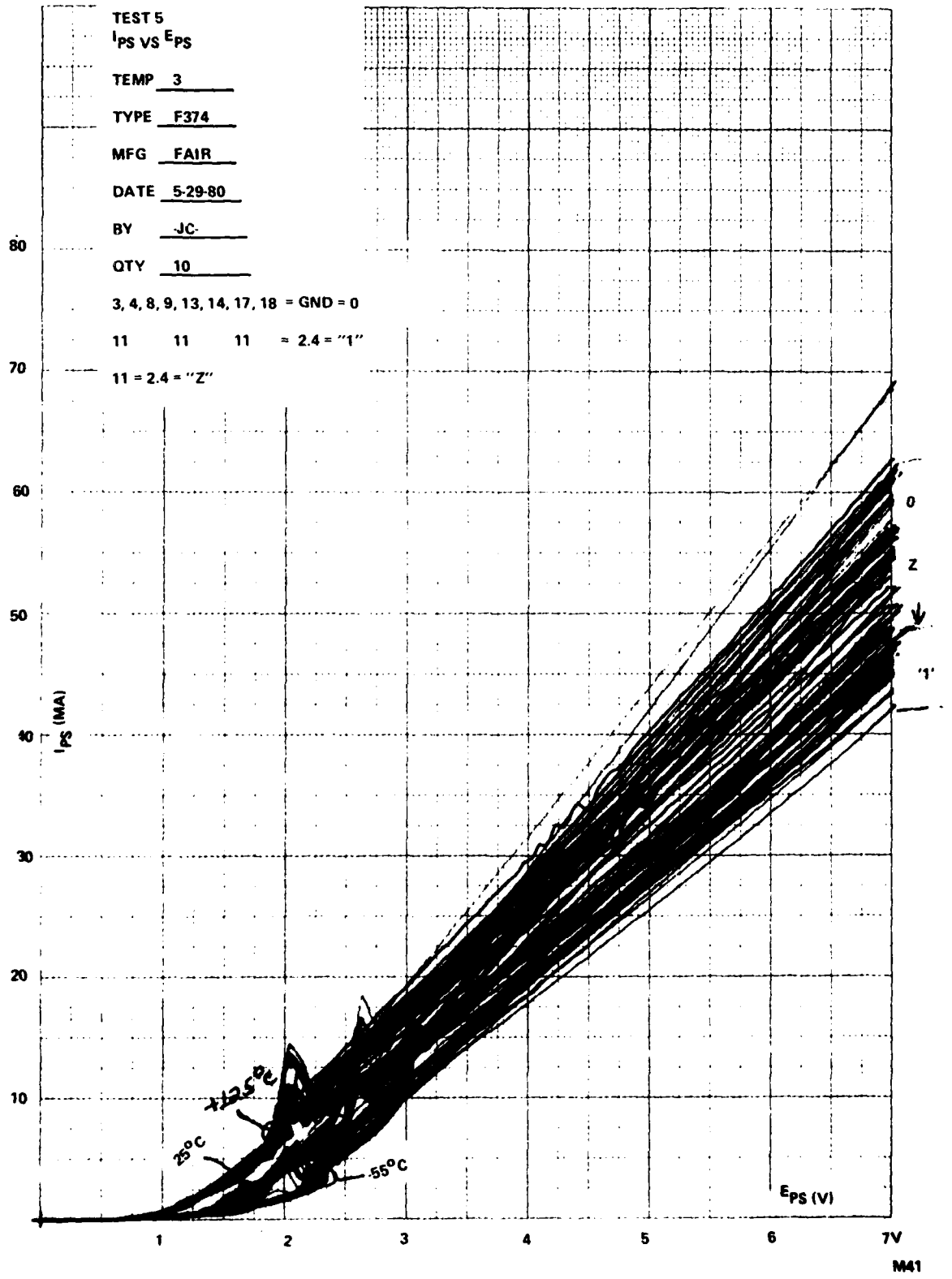

TEST 4A (VCC 5.5V)
I_{IN} VS $E_{IN}(0)$
PIN 1
TEMP 3
TYPE F20
MFR FAIRCHILD
QTY 10
DATE 7-31-80
BY JV
.56
.48
.4
.32
.24
.16
.08
I_{IN}(mA)
+125°C
+25°C
-55° C
$E_{IN(V)}$
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2V
4A M41

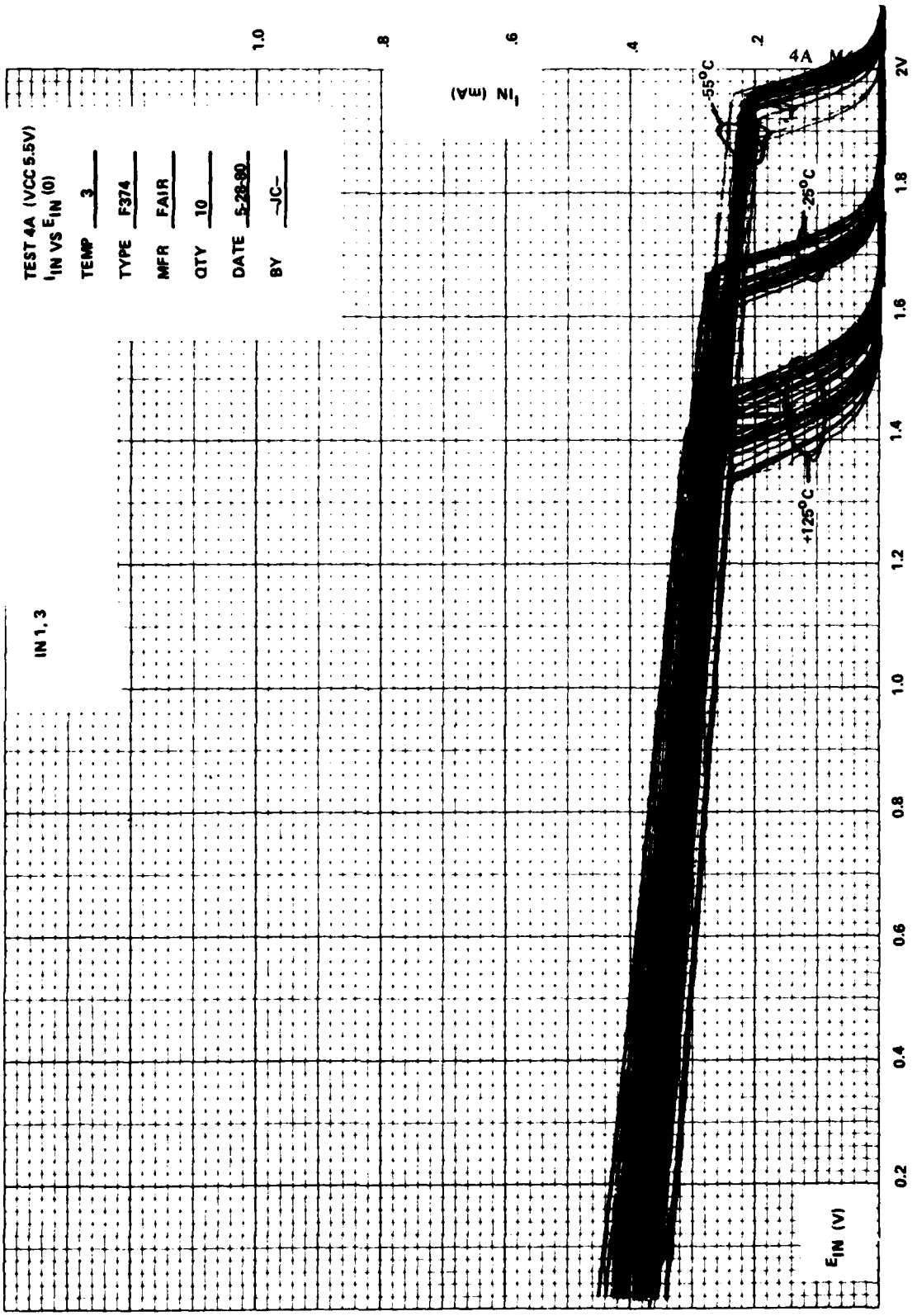

TEST 3 (VCC 4.5V)
E_{OUT} VS E_{IN}
TEMP 3
TYPE F20
MFR FAIRCHILD
DATE 7-31-80
QTY 10
BY JV
IN PIN 1
OUT PIN 6
E_{OUT}(V)
E_{IN}(V)
-55°C
25°C
+125°C
#9
#1

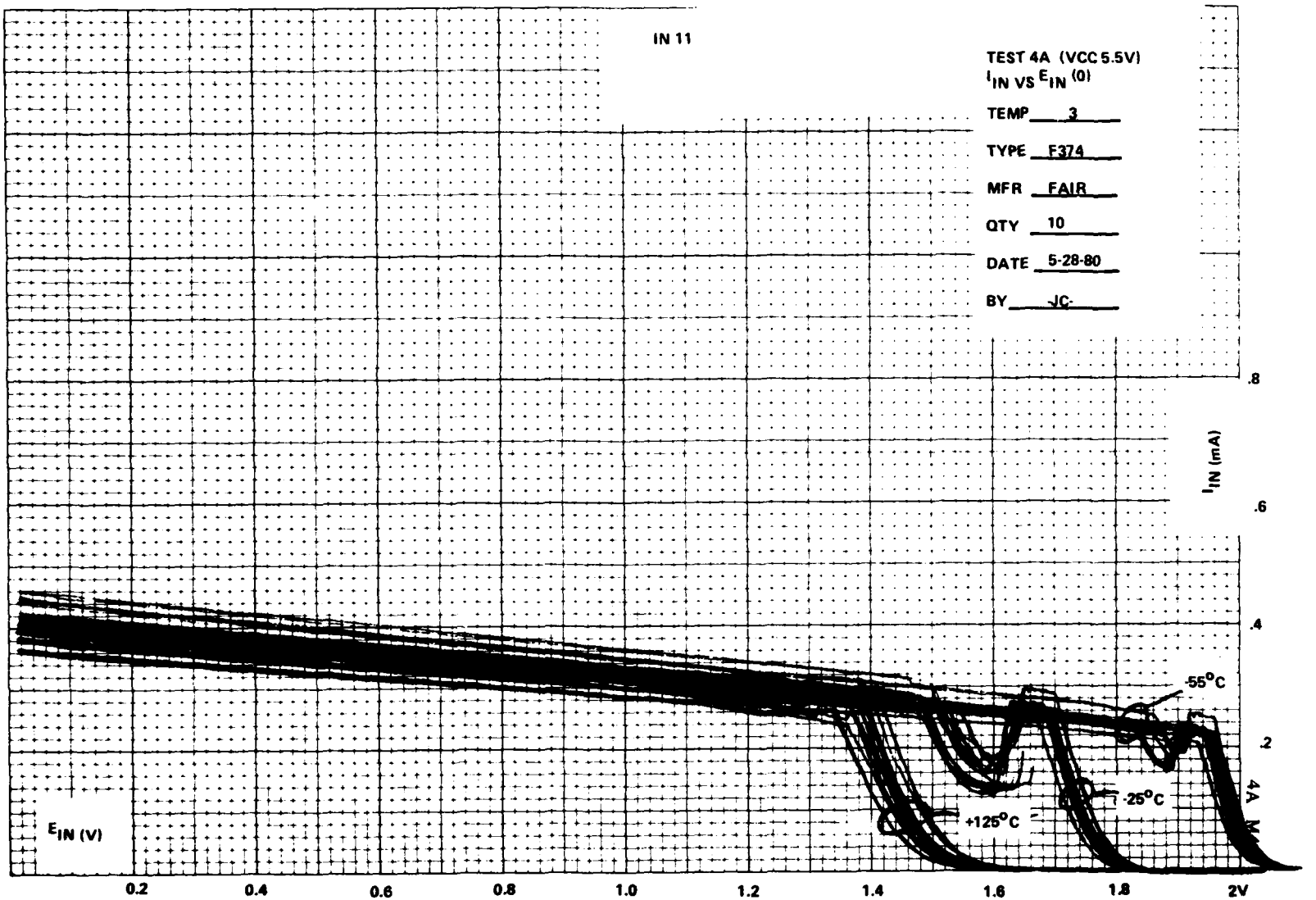

(NOTE: OFFSET "Y" BY +5)
TEST 4B (5.5V)
I_{IN} VS E_{IN}(BKDWN)
TEMP 3
TYPE F20
MFR FAIRCHILD
DATE 7-30-80
BY -JV-
QTY UNITS 10
IN PIN 1
I_{IN}(mA)
+.32
+.24
+.16
+.08
0
-.08
-.16
-.24
-.32
+25° C
-55°C
+125° C
2V
4V
6V
8V
10V
E_{IN}(V)

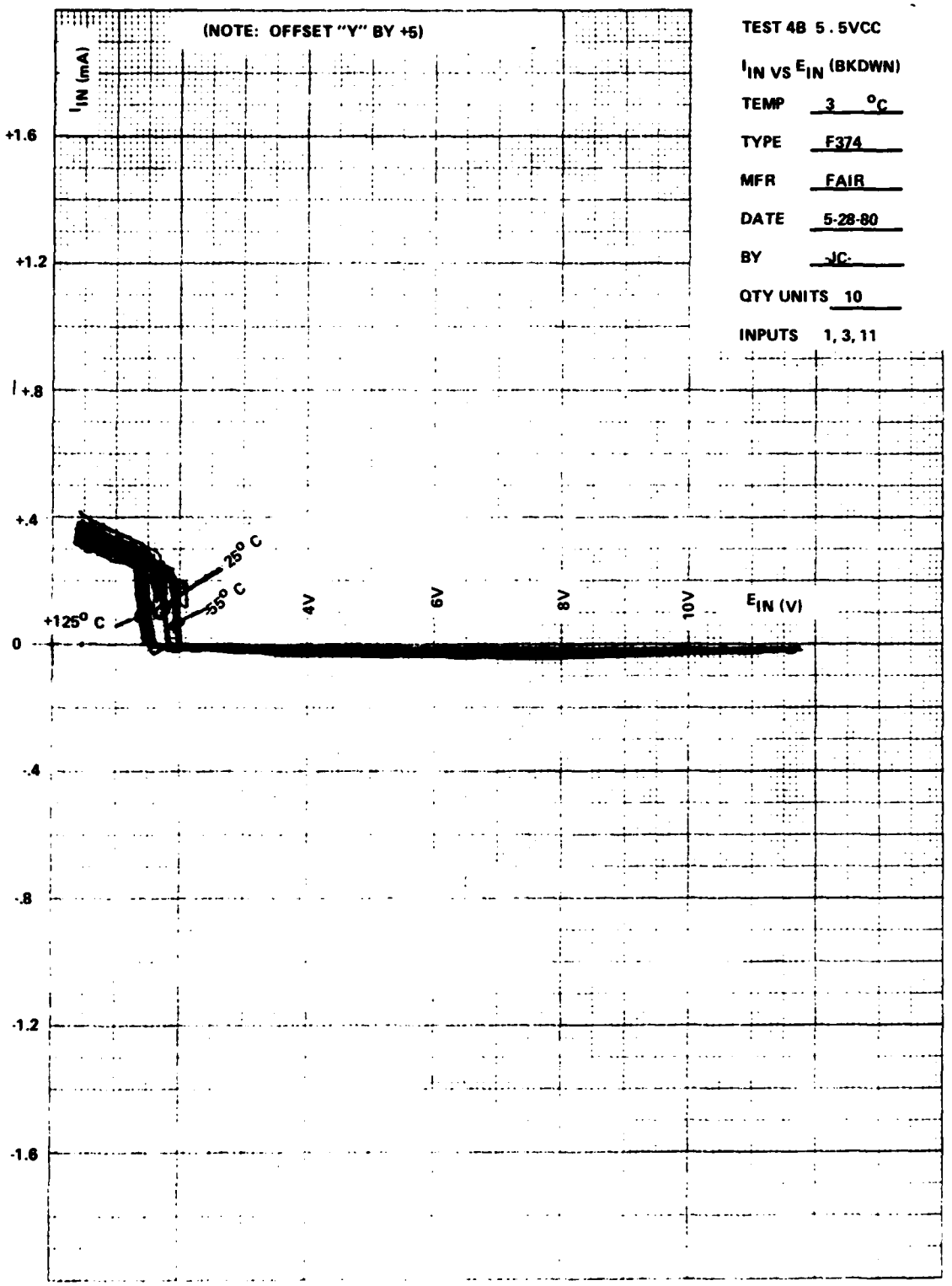

1A M41
TEST 1A (VCC 4.5V)
I_{OUT} VS E_{OUT}(0)
TEMP 3
TYPE F374
MFR FAIR
DATE 5-28-80
QTY 10
BY JC
3, 1 = 7V
11 = 2.4V
OUT 2
160
140
120
100
80
60
40
20
I_{OUT}(mA)
+125°C
25°C
-55°C
0.5
1.0
1.5
2.0
2.5
3.0
3.5V
E_{OUT}(V)

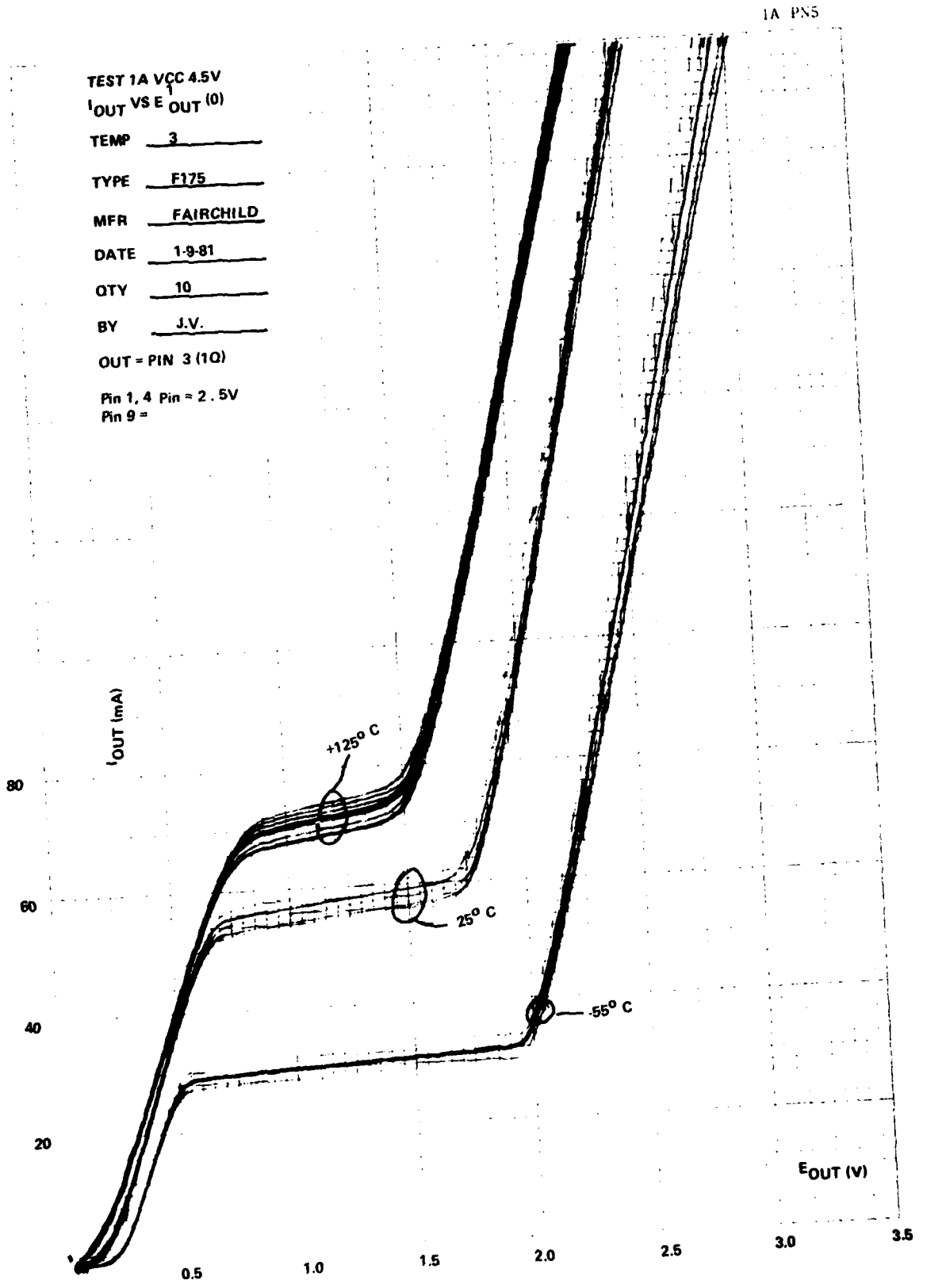

TEST 2 (VCC 5.5V)
IOUT VS EOUT(1)
TEMP 3
TYPE F374
MFR FAIR
DATE 5-28-80
BY JC
QTY 10
1, 11 = GND
3 = 2.4V
OUT 2
100
90
80
70
60
50
40
30
20
10
IOUT(mA)
25°C
+125° C
-55°C
EOUT(V)
1
2
3
4
5
6
7V

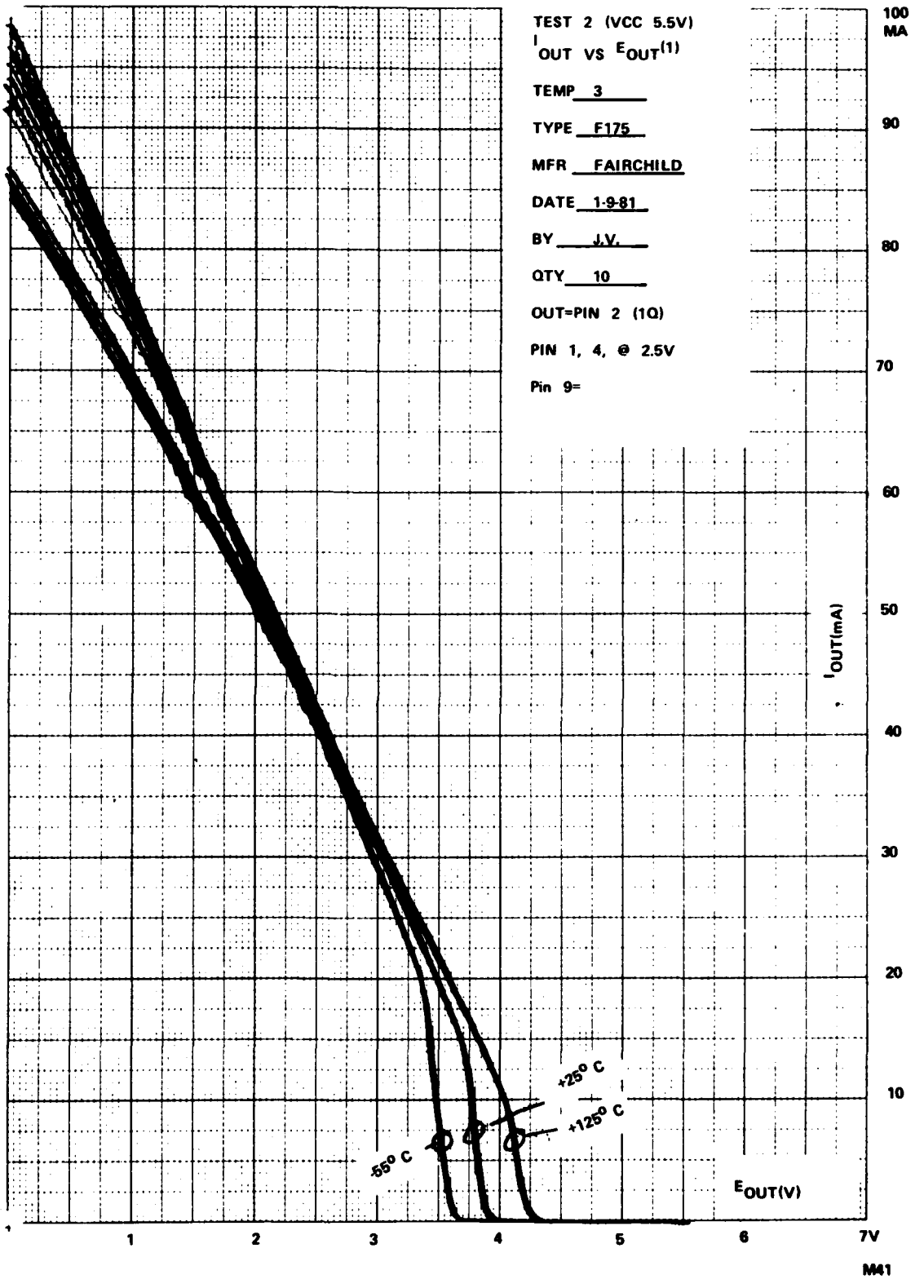

TEST 5
I_{PS} VS E_{PS}
TEMP 3
TYPE F374
MFG FAIR
DATE 5-29-80
BY JC
QTY 10
3, 4, 8, 9, 13, 14, 17, 18 = GND = 0
11 11 11 = 2.4 = "1"
11 = 2.4 = "Z"
80
70
60
50
40
30
20
10
I_{PS} (MA)
0
Z
"1"
+125°C
25°C
-55°C
E_{PS} (V)
1
2
3
4
5
6
7V
M41

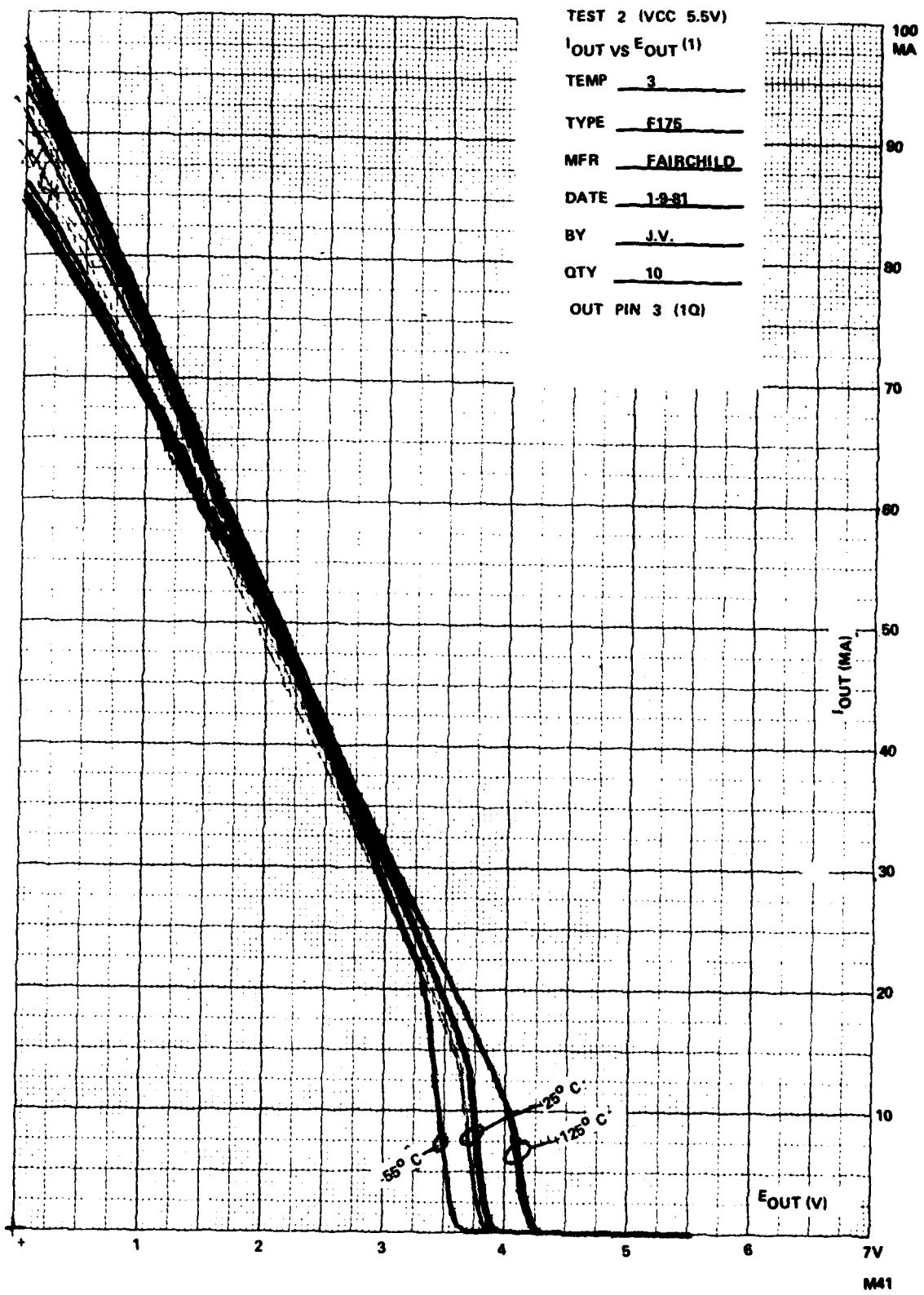

TEST 4A (VCC 5.5V)
I_{IN} VS E_{IN} (0)
TEMP 3
TYPE F374
MFR FAIR
QTY 10
DATE 5-28-80
BY -JC-
IN 1, 3
I_{IN} (mA)
E_{IN} (V)
-55°C
25°C
+125°C
4A


IN 11
TEST 4A (VCC 5.5V)
I_{IN} VS E_{IN} (0)
TEMP 3
TYPE F374
MFR FAIR
QTY 10
DATE 5-28-80
BY JC
I_{IN} (mA)
.8
.6
.4
.2
-55°C
-25°C
+125°C
E_{IN} (V)
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2V

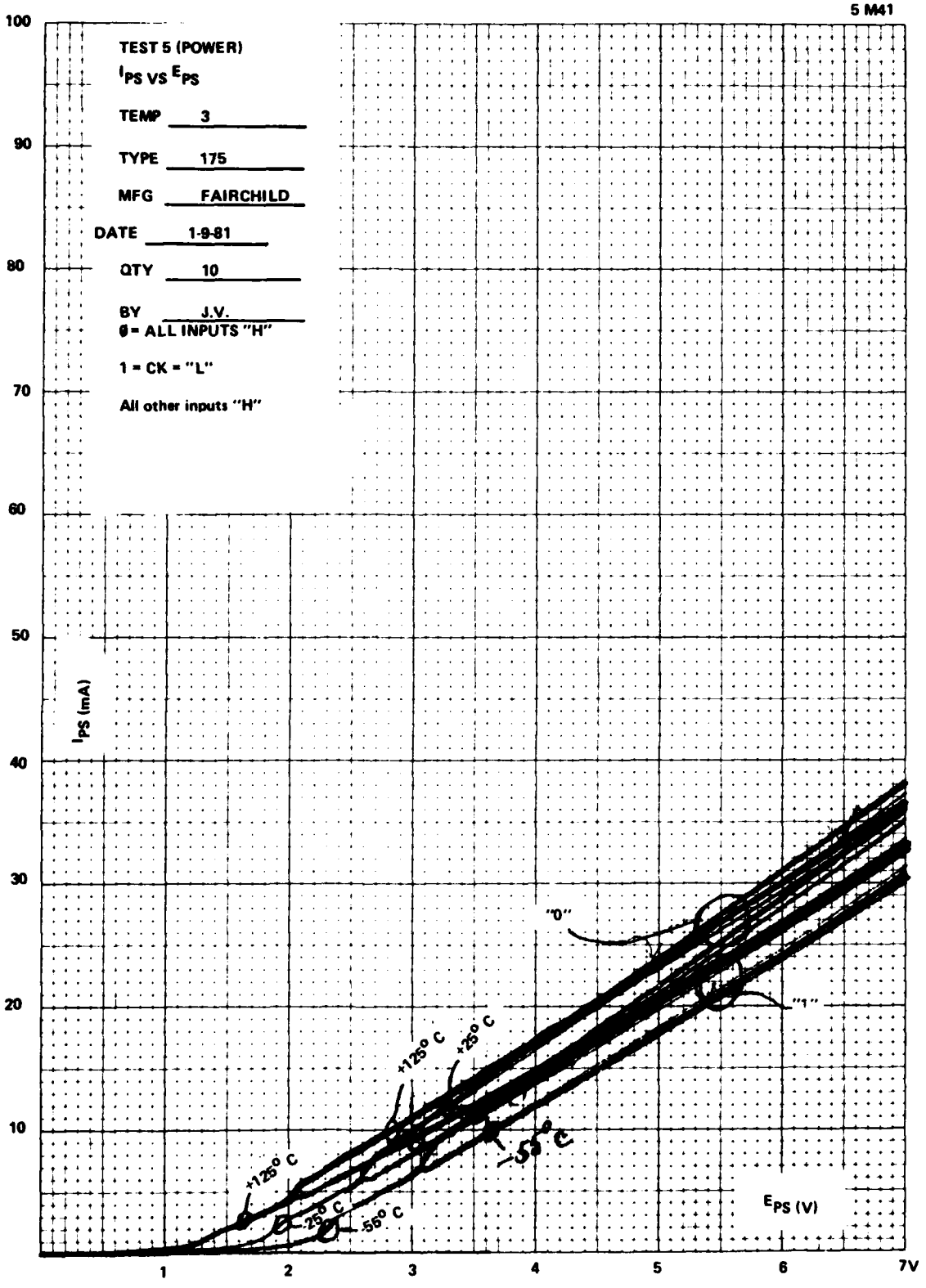

(NOTE: OFFSET "Y" BY +5)
I_{IN} (mA)
+1.6
+1.2
+.8
+.4
0
-.4
-.8
-1.2
-1.6
+125° C
25° C
-55° C
4V
6V
8V
10V
E_{IN} (V)
TEST 4B 5.5VCC
I_{IN} VS E_{IN} (BKDWN)
TEMP 3 °C
TYPE F374
MFR FAIR
DATE 5-28-80
BY JC
QTY UNITS 10
INPUTS 1, 3, 11

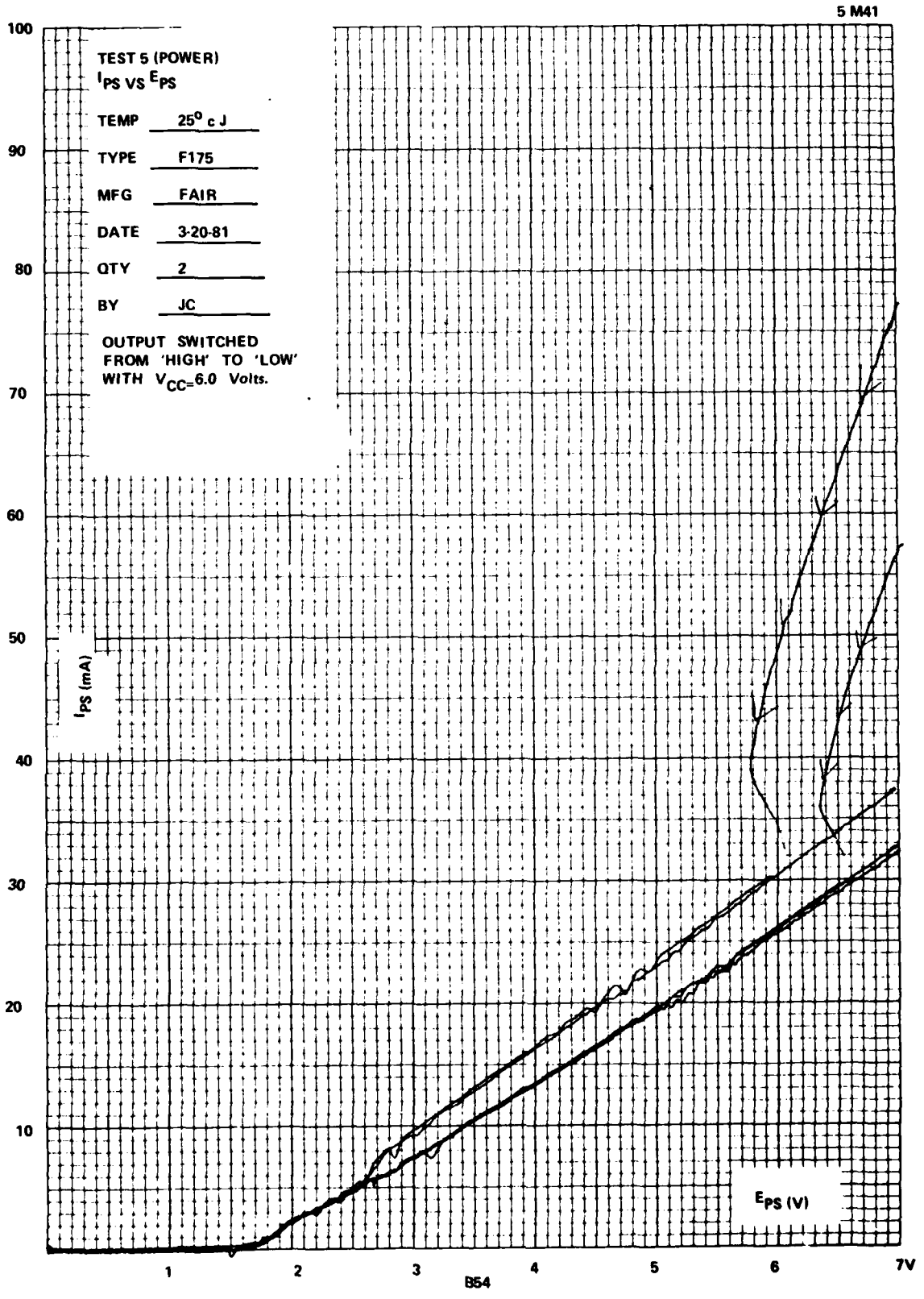

1A PN5
TEST 1A VCC 4.5V
I_{OUT} VS E_{OUT} (0)
TEMP 3
TYPE F175
MFR FAIRCHILD
DATE 1-9-81
QTY 10
BY J.V.
OUT = PIN 3 (1Q)
Pin 1, 4 Pin = 2 . 5V
Pin 9 =
I_{OUT} (mA)
+125° C
25° C
-55° C
80
60
40
20
0.5
1.0
1.5
2.0
2.5
3.0
3.5
E_{OUT} (V)

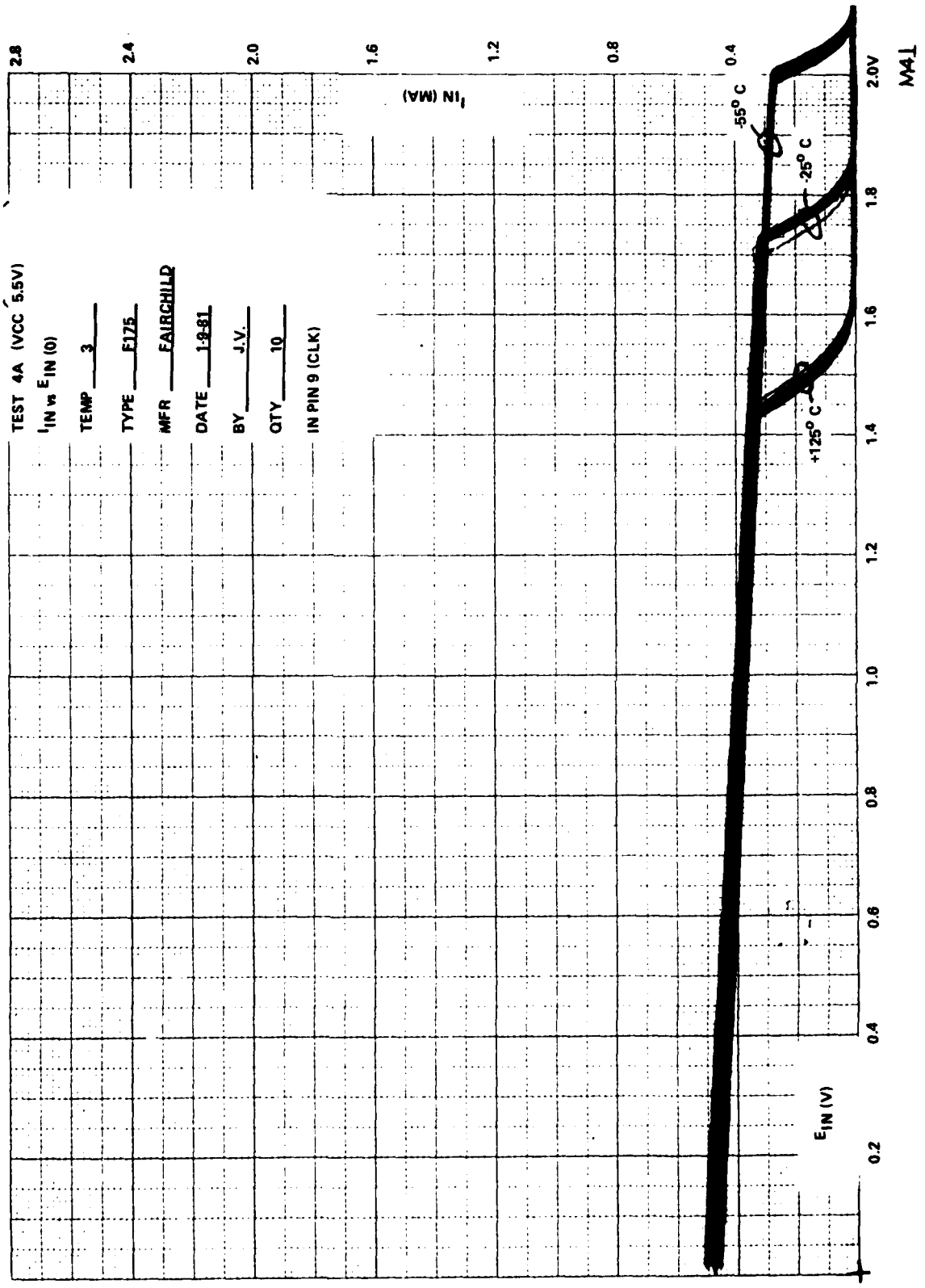

TEST 2 (VCC 5.5V)
I OUT VS E OUT(1)
TEMP 3
TYPE F175
MFR FAIRCHILD
DATE 1-9-81
BY J.V.
QTY 10
OUT=PIN 2 (1Q)
PIN 1, 4, @ 2.5V
Pin 9=
100 MA
90
80
70
60
50
40
30
20
10
I OUT(mA)
+25° C
+125° C
-55° C
E OUT(V)
1
2
3
4
5
6
7V
M41

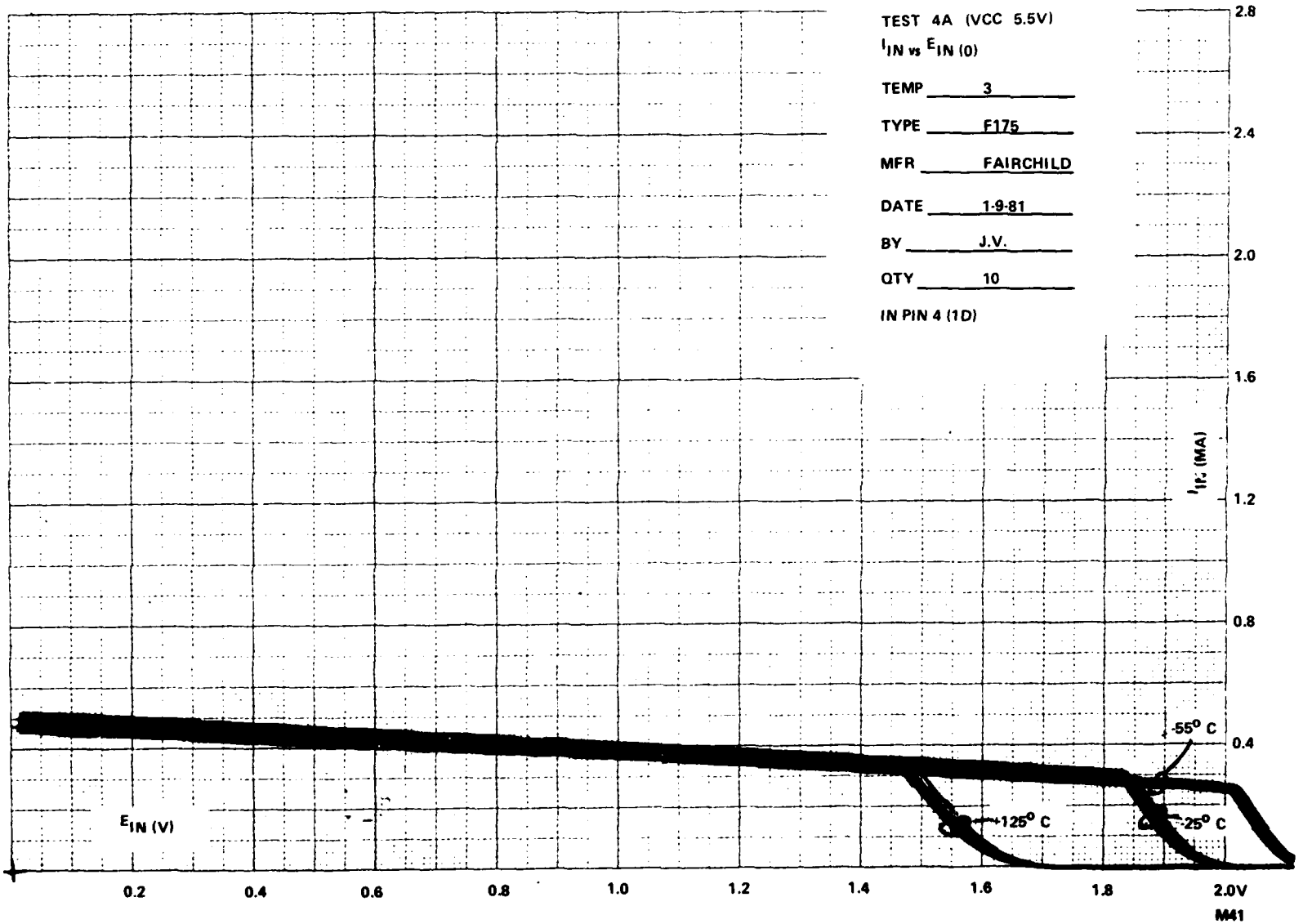

TEST 2 (VCC 5.5V)
I_{OUT} VS E_{OUT} (1)
TEMP 3
TYPE F175
MFR FAIRCHILD
DATE 1-9-81
BY J.V.
QTY 10
OUT PIN 3 (1Q)
100 MA
90
80
70
60
50
40
30
20
10
I_{OUT} (MA)
-55° C
25° C
125° C
E_{OUT} (V)
+
1
2
3
4
5
6
7V
M41

5 M41

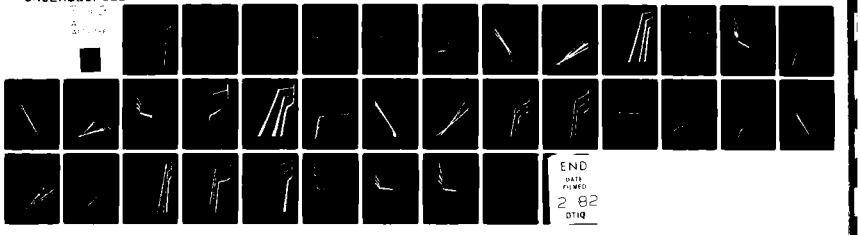

TEST 5 (POWER)
I_{PS} VS E_{PS}
TEMP 3
TYPE 175
MFG FAIRCHILD
DATE 1-9-81
QTY 10
BY J.V.
0 = ALL INPUTS "H"
1 = CK = "L"
All other inputs "H"
I_{PS} (mA)
E_{PS} (V)
"0"
"1"
+125° C
+25° C
-55° C
+125° C
-25° C
-55° C
100
90
80
70
60
50
40
30
20
10
1
2
3
4
5
6
7V

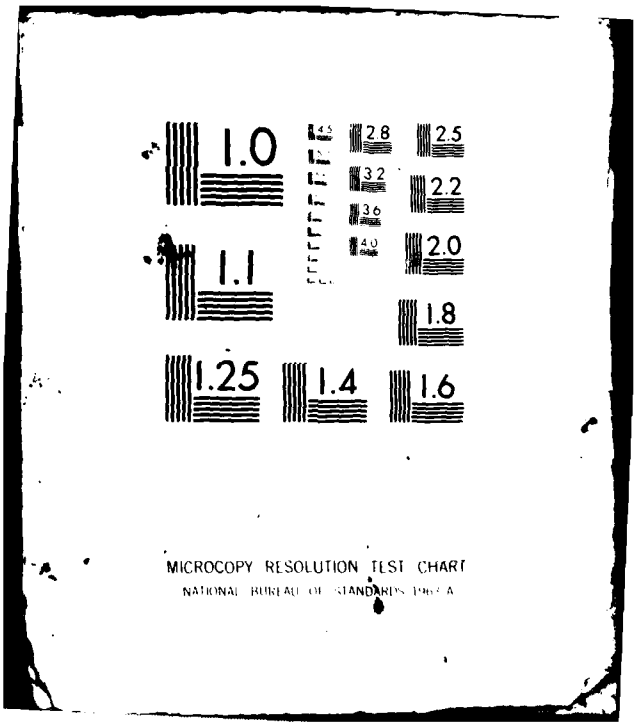

5 M41
TEST 5 (POWER)
I_{PS} VS E_{PS}
TEMP 25° c J
TYPE F175
MFG FAIR
DATE 3-20-81
QTY 2
BY JC
OUTPUT SWITCHED FROM 'HIGH' TO 'LOW' WITH V_{CC}=6.0 Volts.
I_{PS} (mA)
100
90
80
70
60
50
40
30
20
10
1
2
3
4
5
6
7V
E_{PS} (V)
B54

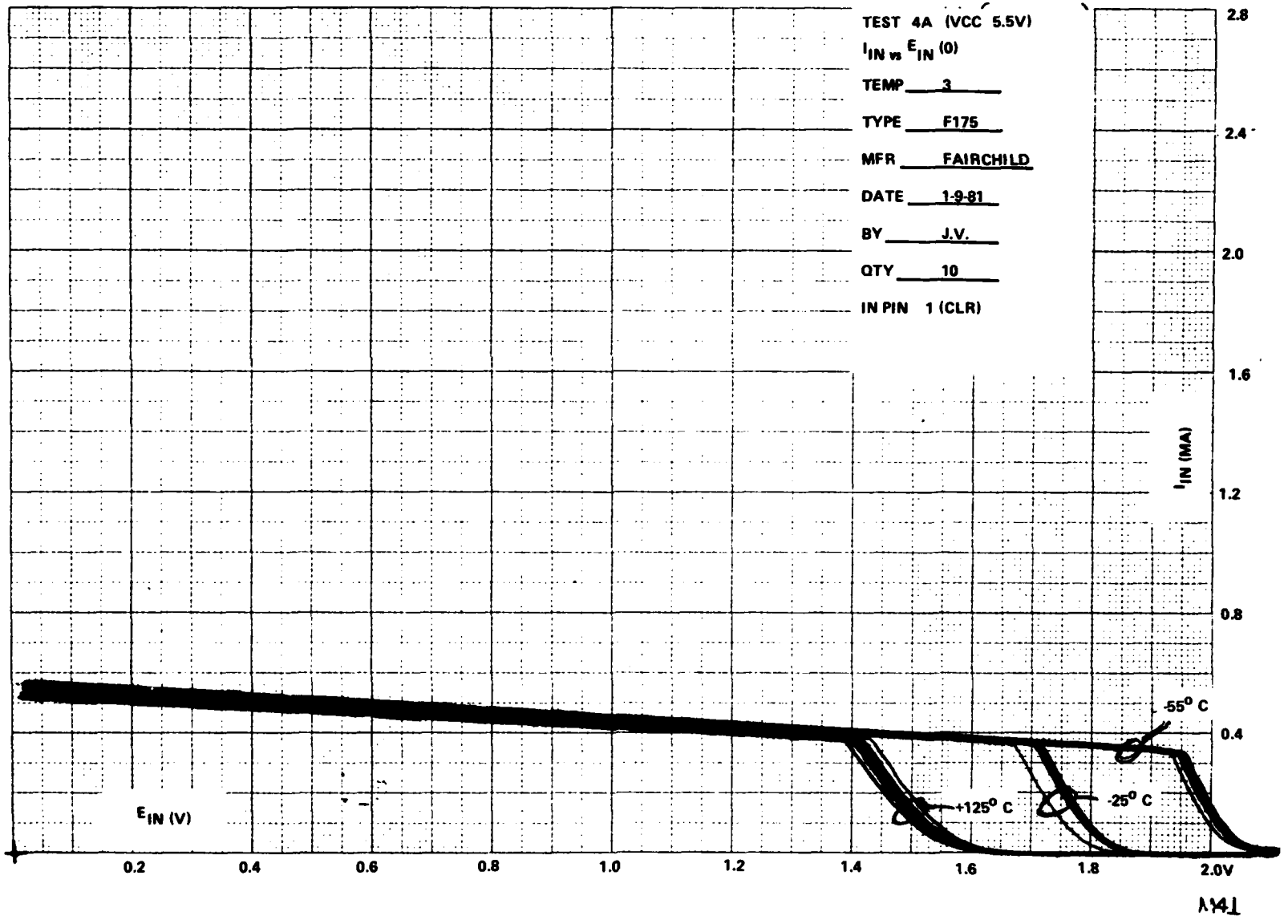

TEST 4A (VCC 5.5V)
I_{IN} vs E_{IN} (0)
TEMP 3
TYPE F175
MFR FAIRCHILD
DATE 1-9-81
BY J.V.
QTY 10
IN PIN 9 (CLK)
I_{IN} (MA)
E_{IN} (V)
-55° C
-25° C
+125° C
M4L

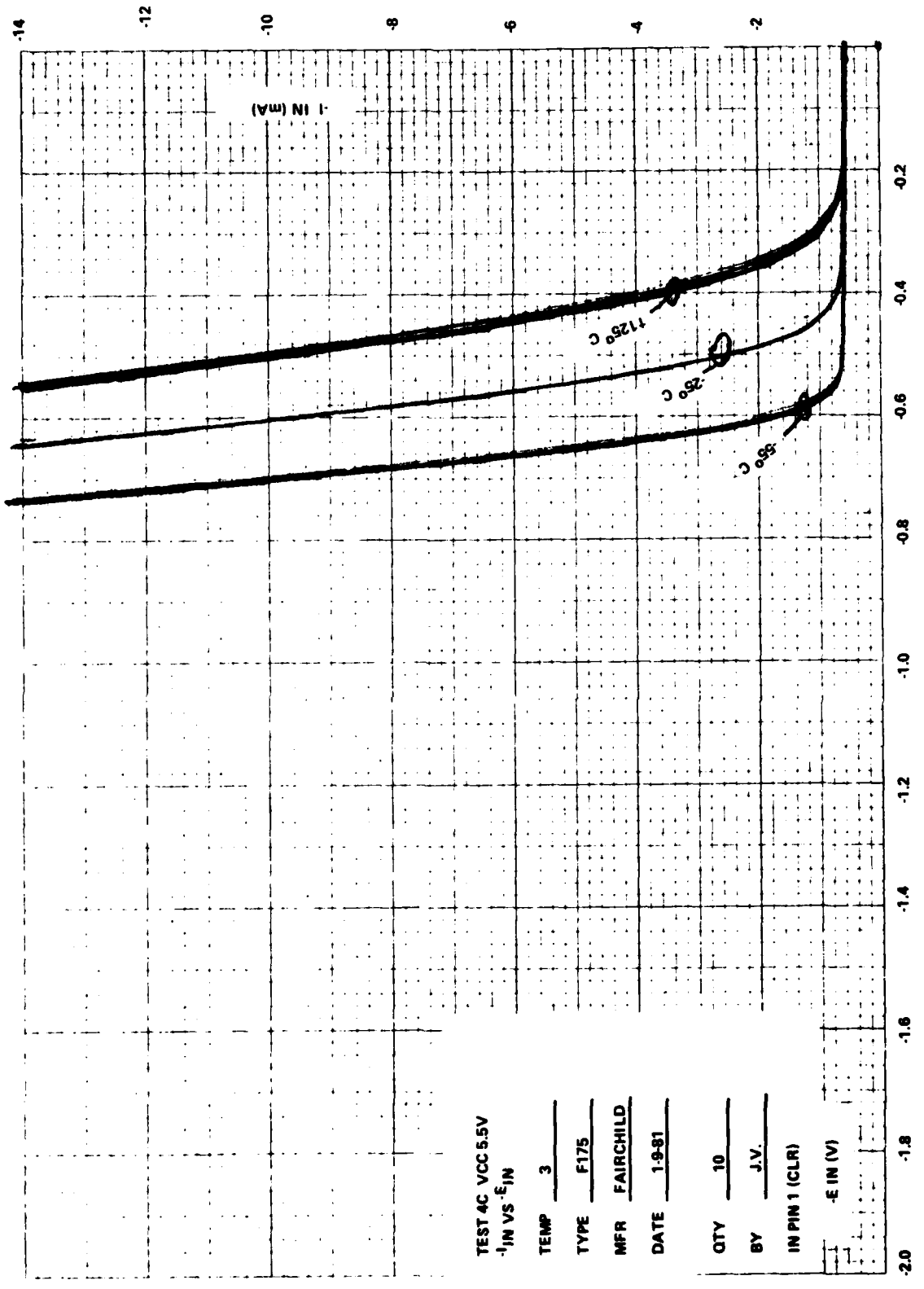

TEST 4A (VCC 5.5V)
I_{IN} vs E_{IN} (0)
TEMP 3
TYPE F175
MFR FAIRCHILD
DATE 1-9-81
BY J.V.
QTY 10
IN PIN 4 (1D)
I_{IN} (MA)
2.8
2.4
2.0
1.6
1.2
0.8
0.4
E_{IN} (V)
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0V
M41
-55° C
+125° C
+25° C

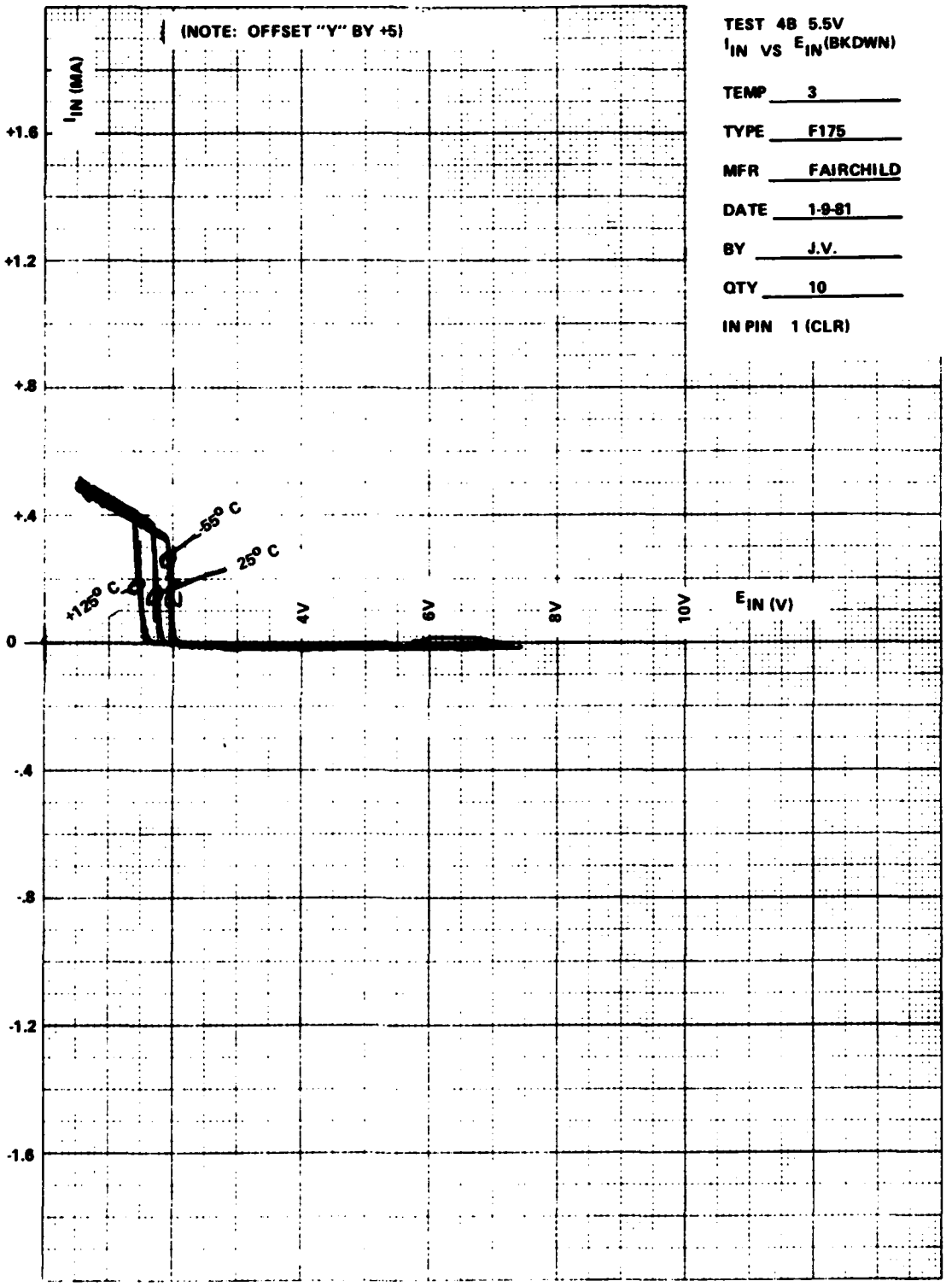
AD-A108 766 IBM FEDERAL SYSTEMS DIV MANASSAS VA F/G 9/1
ELECTRICAL CHARACTERIZATION OF SUPER SCHOTTKY.(U)
JUL 81 R A LAWRENCE F30602-80-C-0068
UNCLASSIFIED RADC-TR-81-194 NL

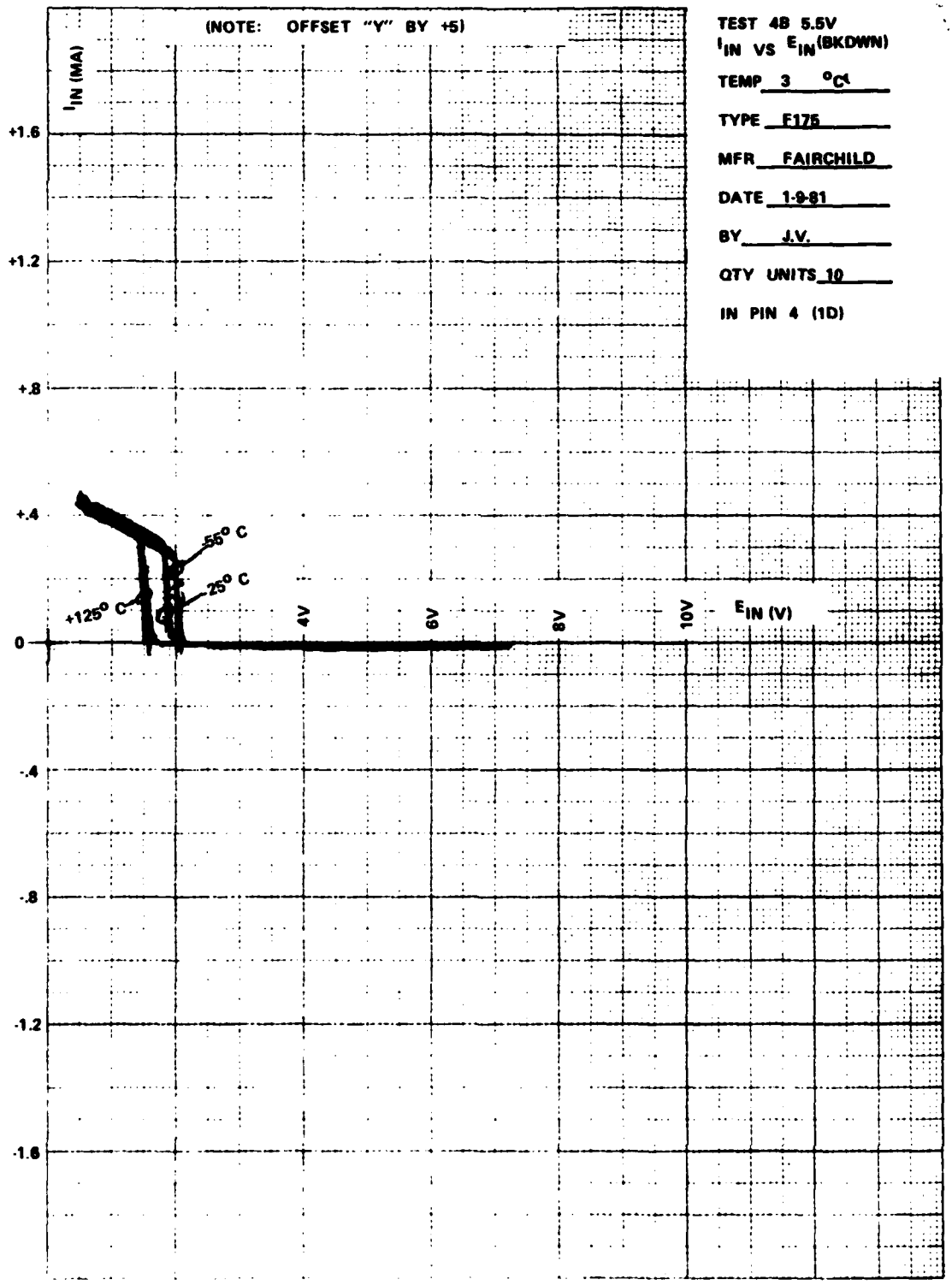


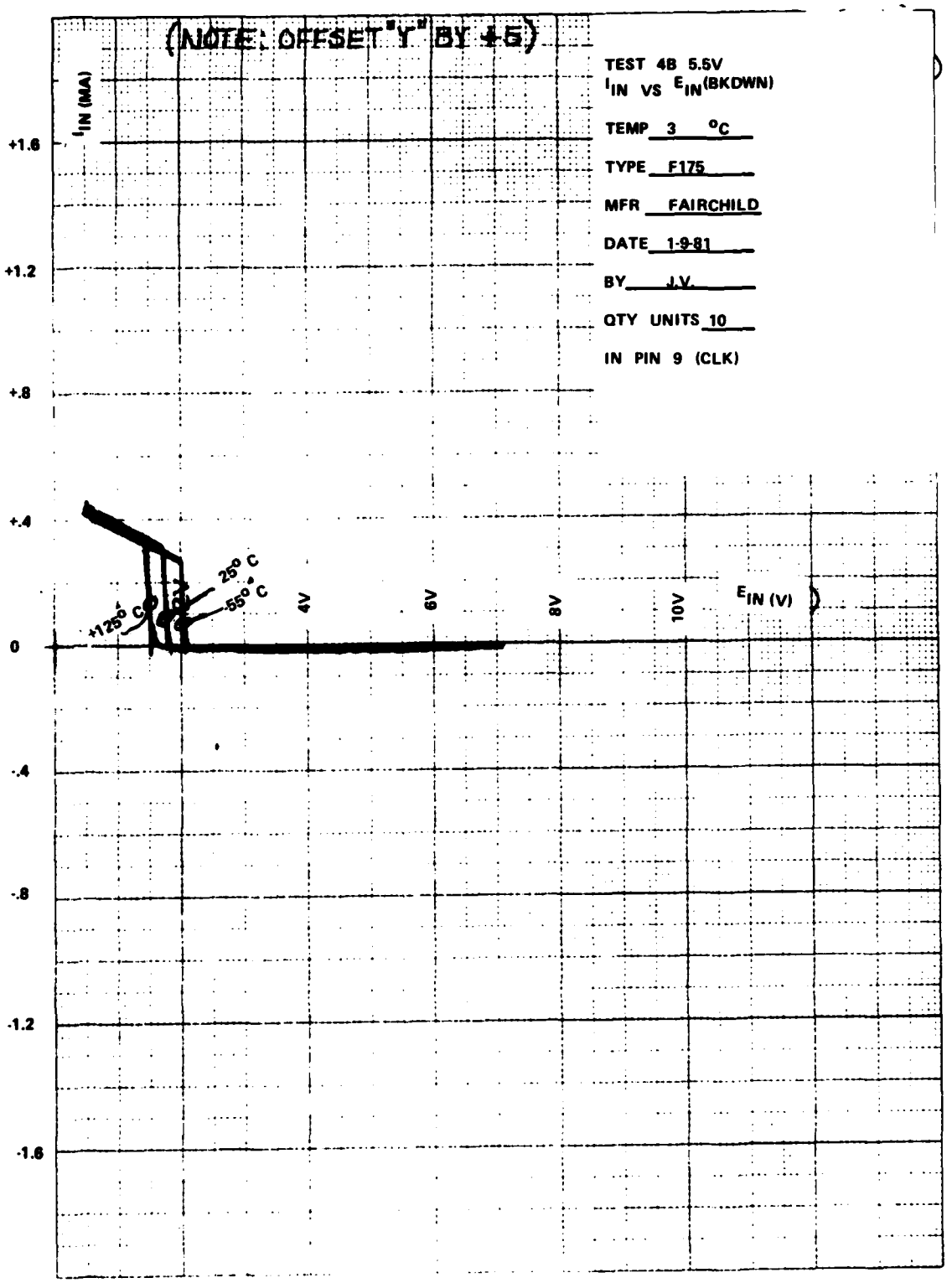

1.0
1.1
1.25
1.4
1.6
2.8
3.2
3.6
4.0
2.5
2.2
2.0
1.8
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A

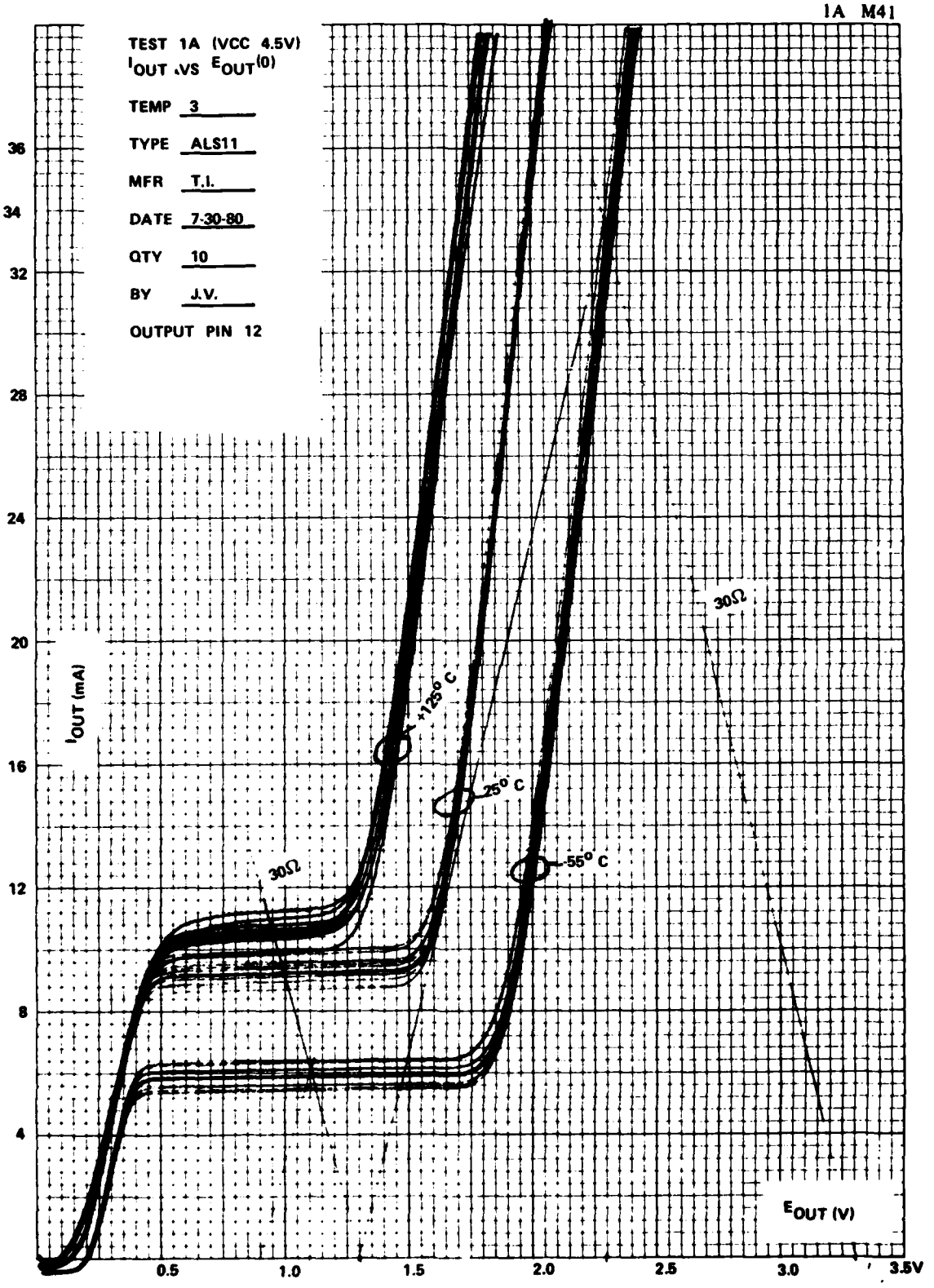

TEST 4A (VCC 5.5V)
I_{IN} vs E_{IN} (0)
TEMP 3
TYPE F175
MFR FAIRCHILD
DATE 1-9-81
BY J.V.
QTY 10
IN PIN 1 (CLR)
I_{IN} (MA)
2.8
2.4
2.0
1.6
1.2
0.8
0.4
E_{IN} (V)
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0V
-55° C
+125° C
-25° C

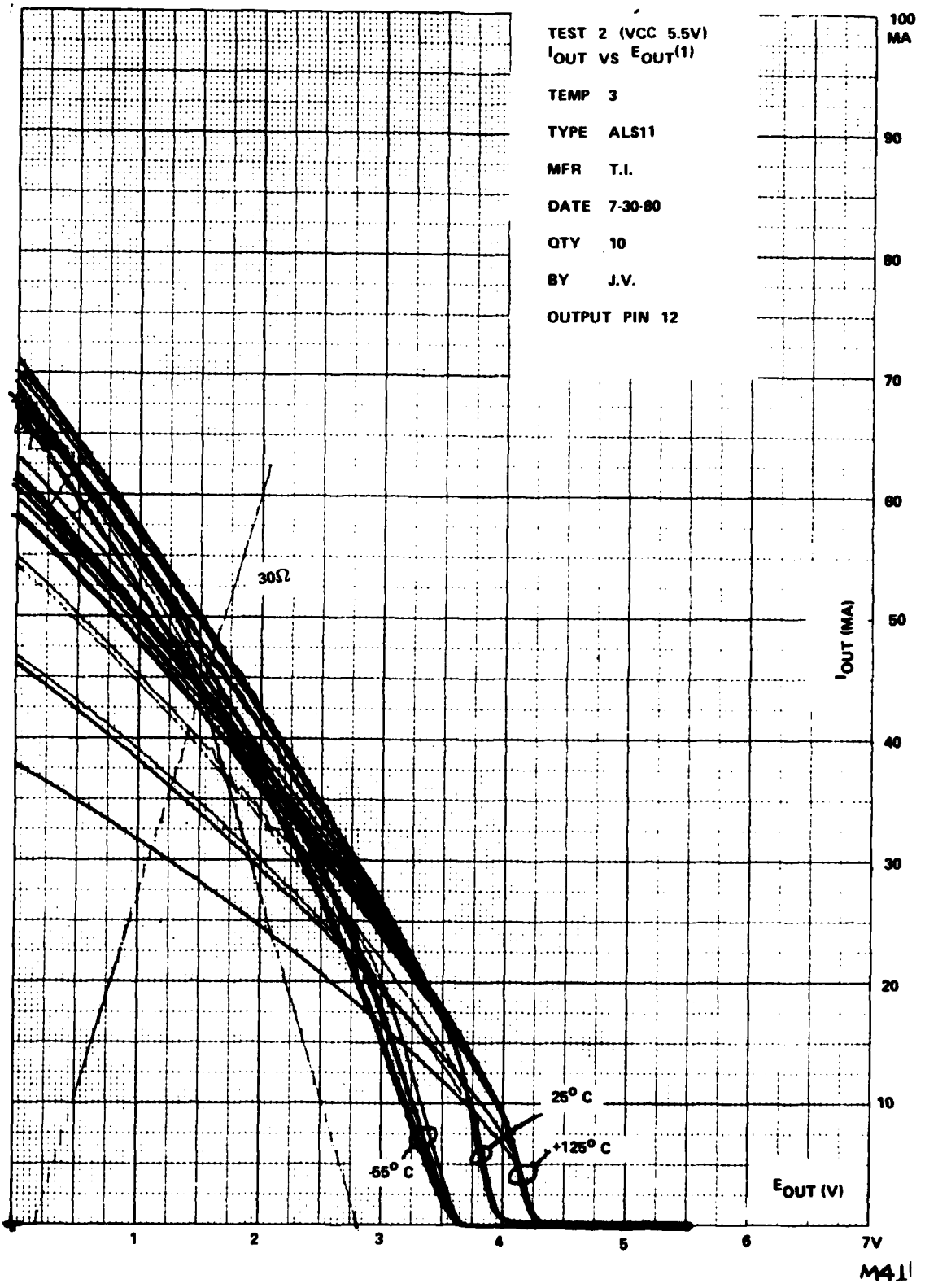

-I IN (mA)
-14
-12
-10
-8
-6
-4
-2
-0.2
-0.4
-0.6
-0.8
-1.0
-1.2
-1.4
-1.6
-1.8
-2.0
-E IN (V)
125° C
25° C
-55° C
TEST 4C VCC 5.5V
-I_IN VS -E_IN
TEMP 3
TYPE F175
MFR FAIRCHILD
DATE 1-9-81
QTY 10
BY J.V.
IN PIN 1 (CLR)


(NOTE: OFFSET "Y" BY +5)
I_{IN} (MA)
+1.6
+1.2
+.8
+.4
0
-.4
-.8
-1.2
-1.6
-55° C
25° C
+125° C
4V
6V
8V
10V
E_{IN} (V)
TEST 4B 5.5V
I_{IN} VS E_{IN}(BKDWN)
TEMP 3
TYPE F175
MFR FAIRCHILD
DATE 1-9-81
BY J.V.
QTY 10
IN PIN 1 (CLR)

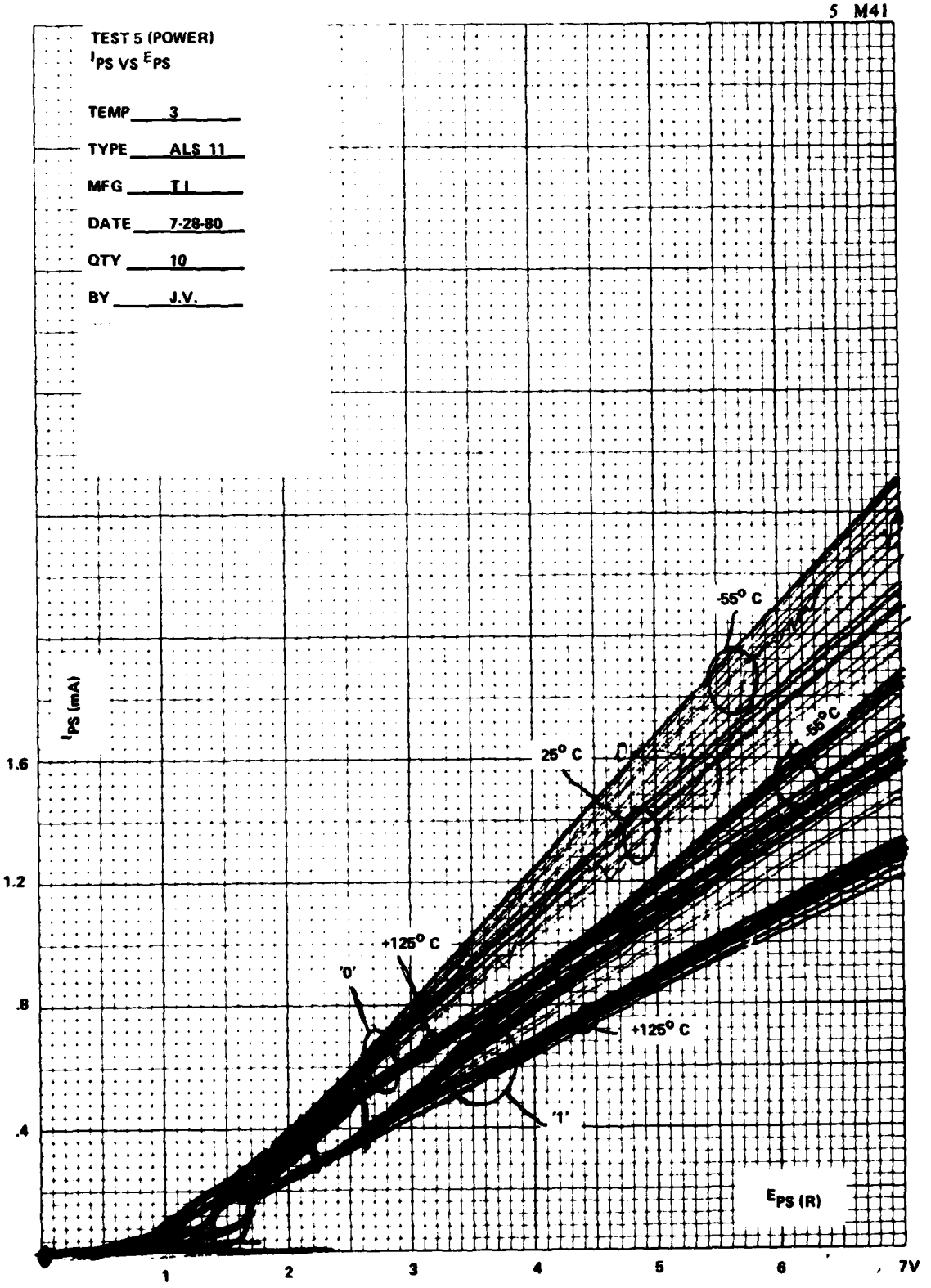

(NOTE: OFFSET "Y" BY +5)
I_{IN} (MA)
+1.6
+1.2
+.8
+.4
0
-.4
-.8
-1.2
-1.6
4V
6V
8V
10V
E_{IN} (V)
+125° C
-55° C
25° C
TEST 4B 5.5V
I_{IN} VS E_{IN}(BKDWN)
TEMP 3 °C
TYPE F175
MFR FAIRCHILD
DATE 1-9-81
BY J.V.
QTY UNITS 10
IN PIN 4 (1D)

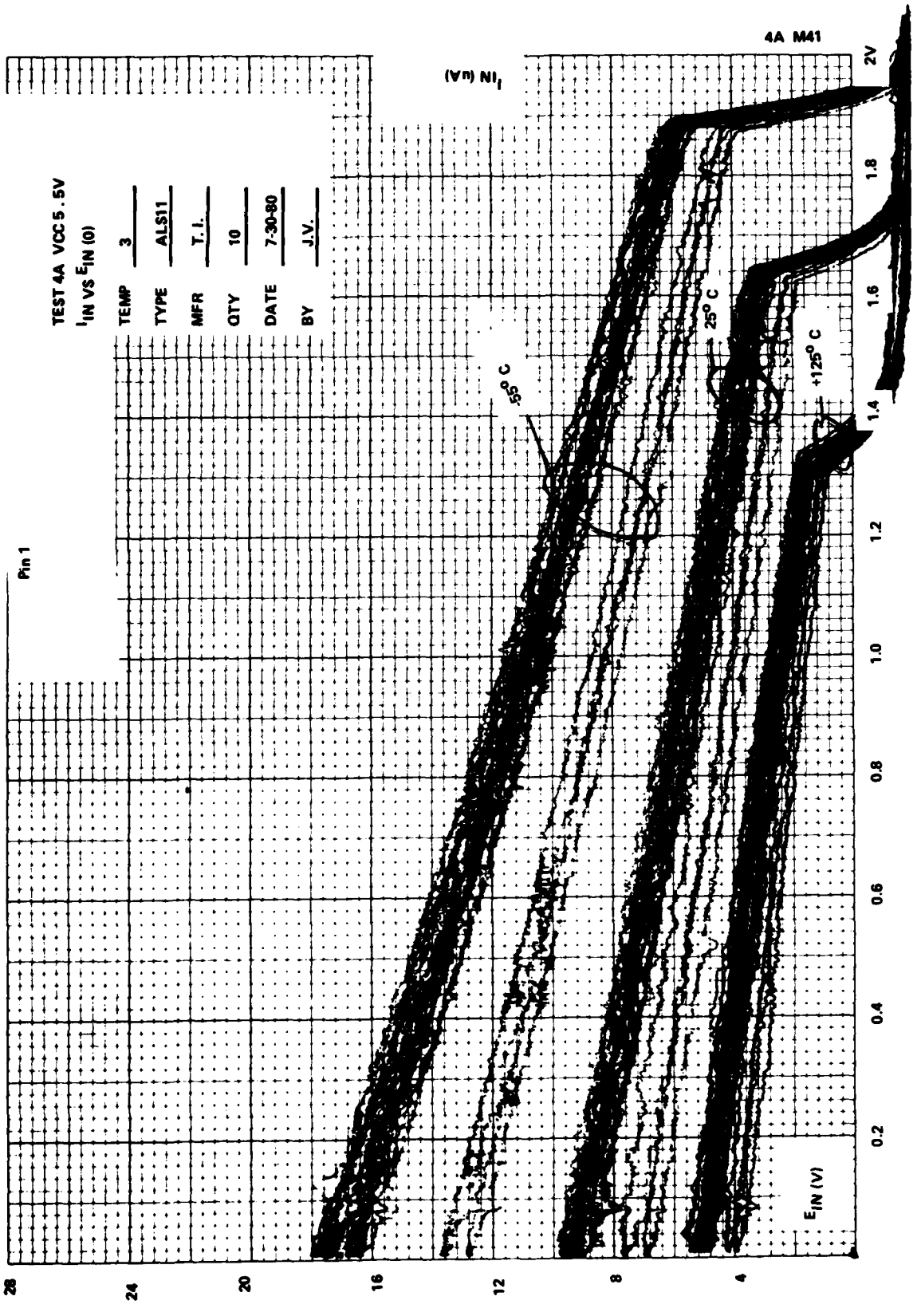

(NOTE: OFFSET "Y" BY +5)
TEST 4B 5.5V
I_{IN} VS E_{IN}(BKDWN)
TEMP 3 °C
TYPE F175
MFR FAIRCHILD
DATE 1-9-81
BY J.V.
QTY UNITS 10
IN PIN 9 (CLK)
I_{IN} (MA)
+1.6
+1.2
+.8
+.4
0
-.4
-.8
-1.2
-1.6
4V
6V
8V
10V
E_{IN} (V)
+125° C
25° C
-55° C

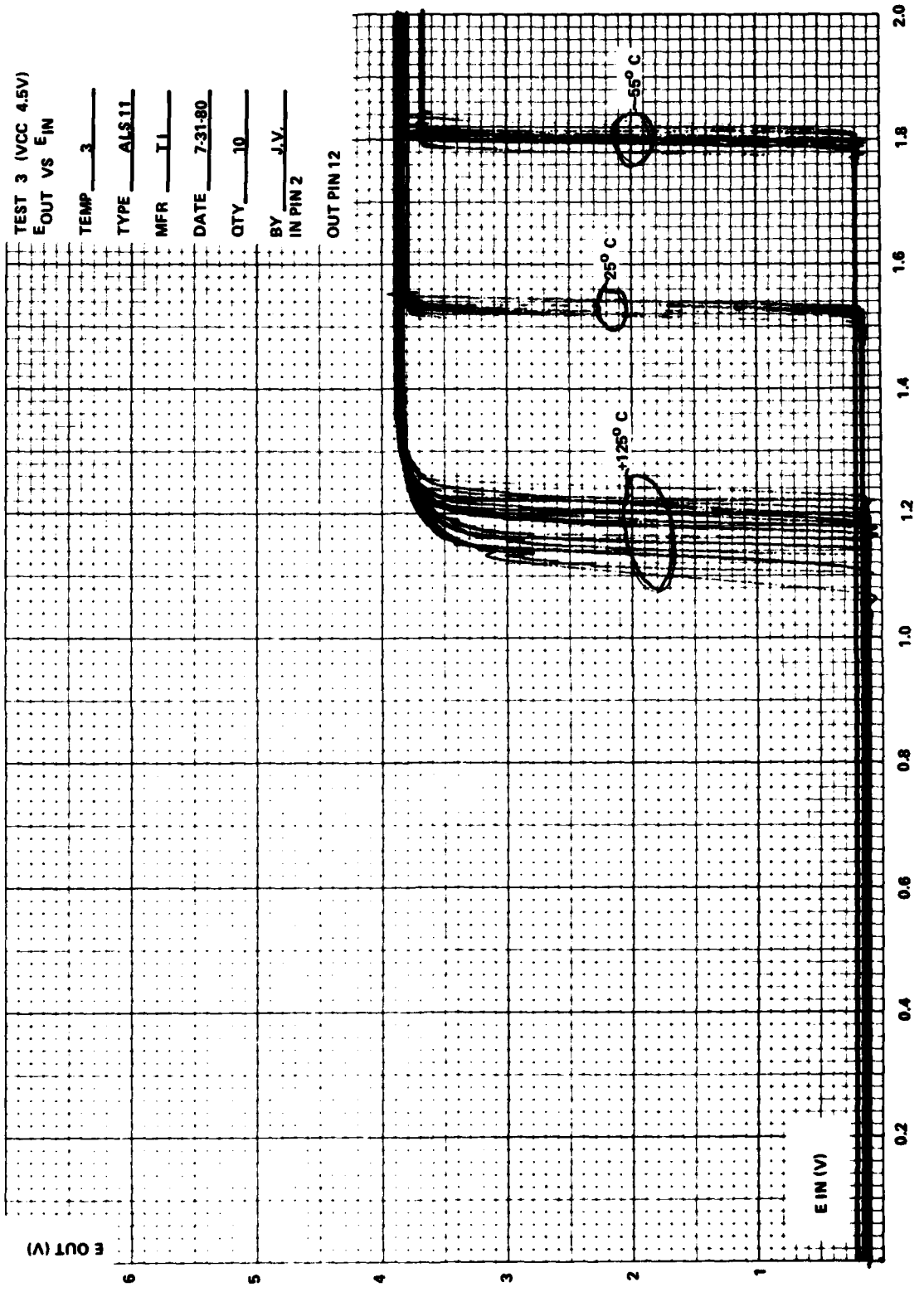

1A M41
TEST 1A (VCC 4.5V)
I_{OUT} vs E_{OUT}(0)
TEMP 3
TYPE ALS11
MFR T.I.
DATE 7-30-80
QTY 10
BY J.V.
OUTPUT PIN 12
36
34
32
28
24
20
16
12
8
4
I_{OUT} (mA)
+125° C
25° C
-55° C
30Ω
30Ω
0.5
1.0
1.5
2.0
2.5
3.0
3.5V
E_{OUT} (V)

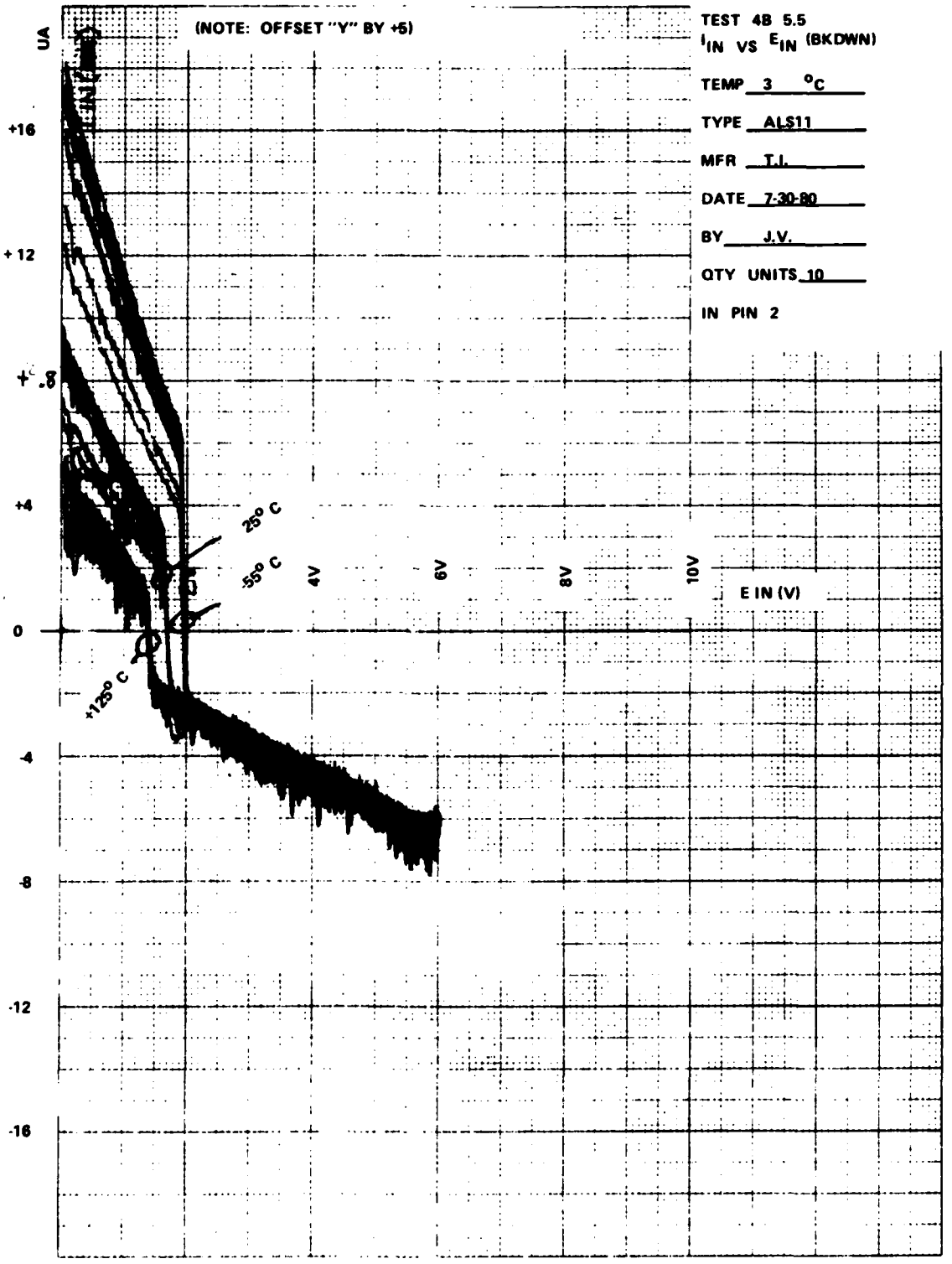

TEST 2 (VCC 5.5V)
I_{OUT} VS E_{OUT}(1)
TEMP 3
TYPE ALS11
MFR T.I.
DATE 7-30-80
QTY 10
BY J.V.
OUTPUT PIN 12
30Ω
25° C
+125° C
-55° C
I_{OUT} (MA)
E_{OUT} (V)
100 MA
90
80
70
60
50
40
30
20
10
1
2
3
4
5
6
7V

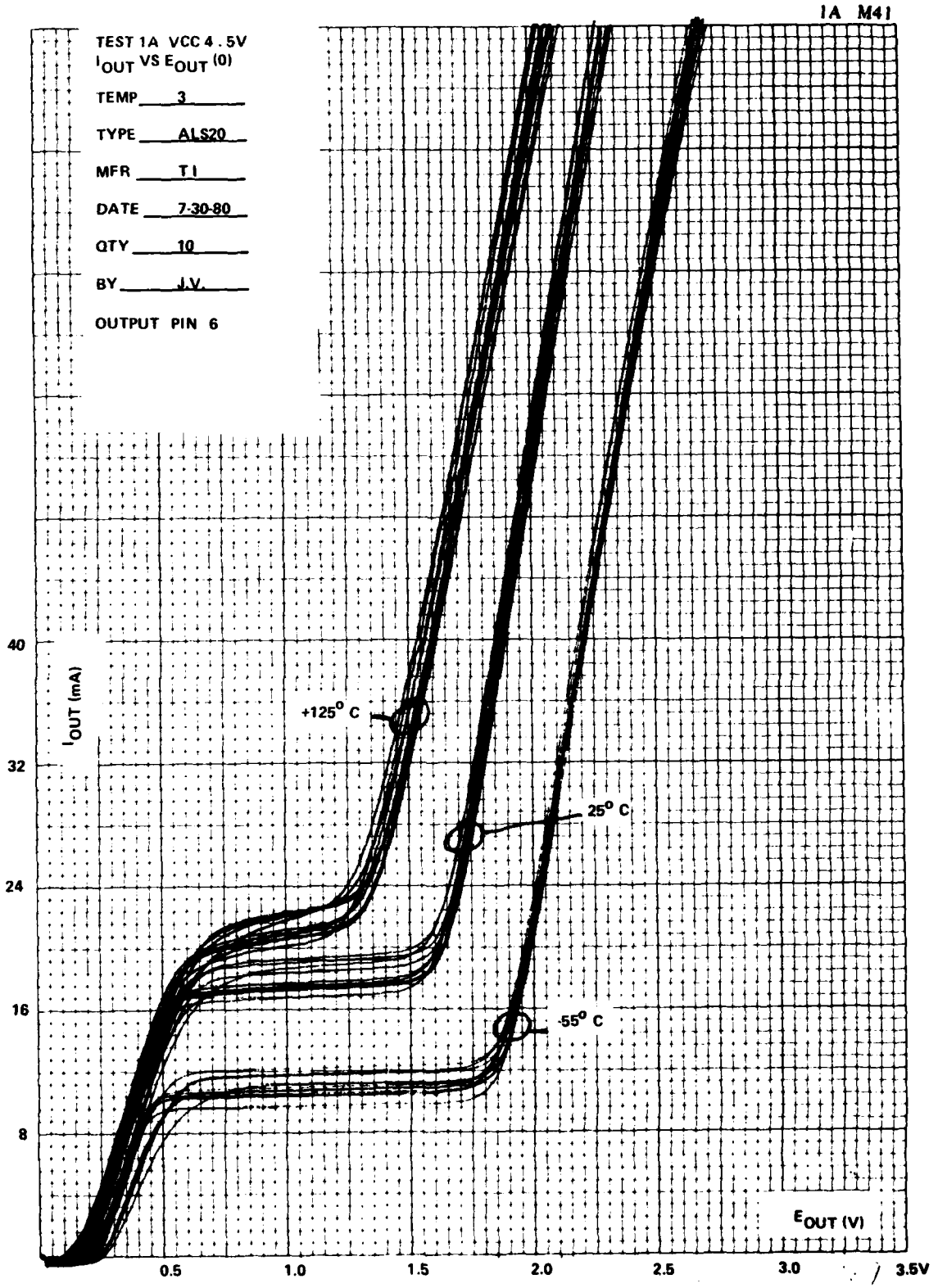
M41

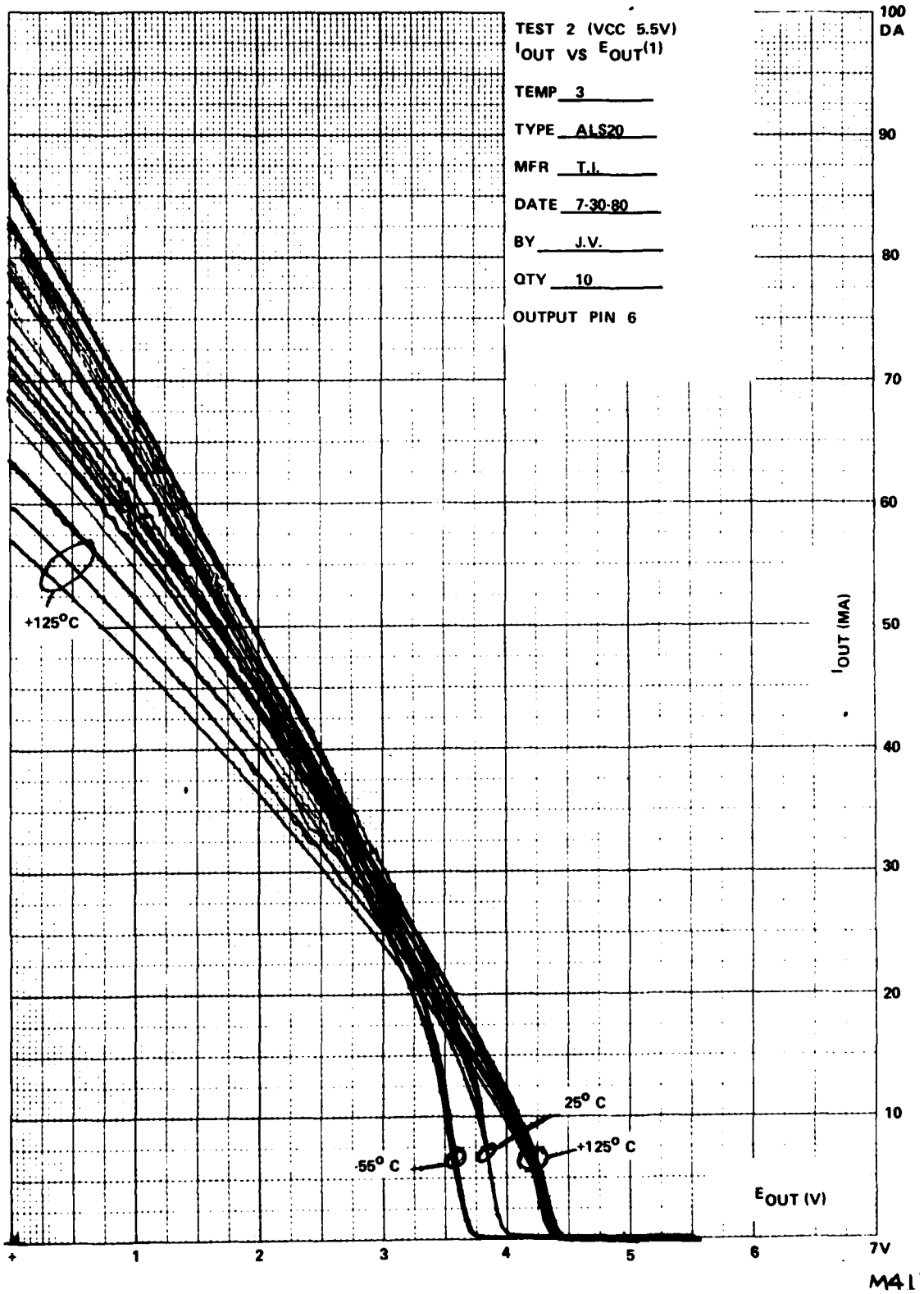

TEST 5 (POWER)
I_{PS} VS E_{PS}
TEMP 3
TYPE ALS 11
MFG TI
DATE 7-28-80
QTY 10
BY J.V.
I_{PS} (mA)
1.6
1.2
.8
.4
-55° C
25° C
+125° C
'0'
+125° C
'1'
E_{PS} (R)
1
2
3
4
5
6
7V

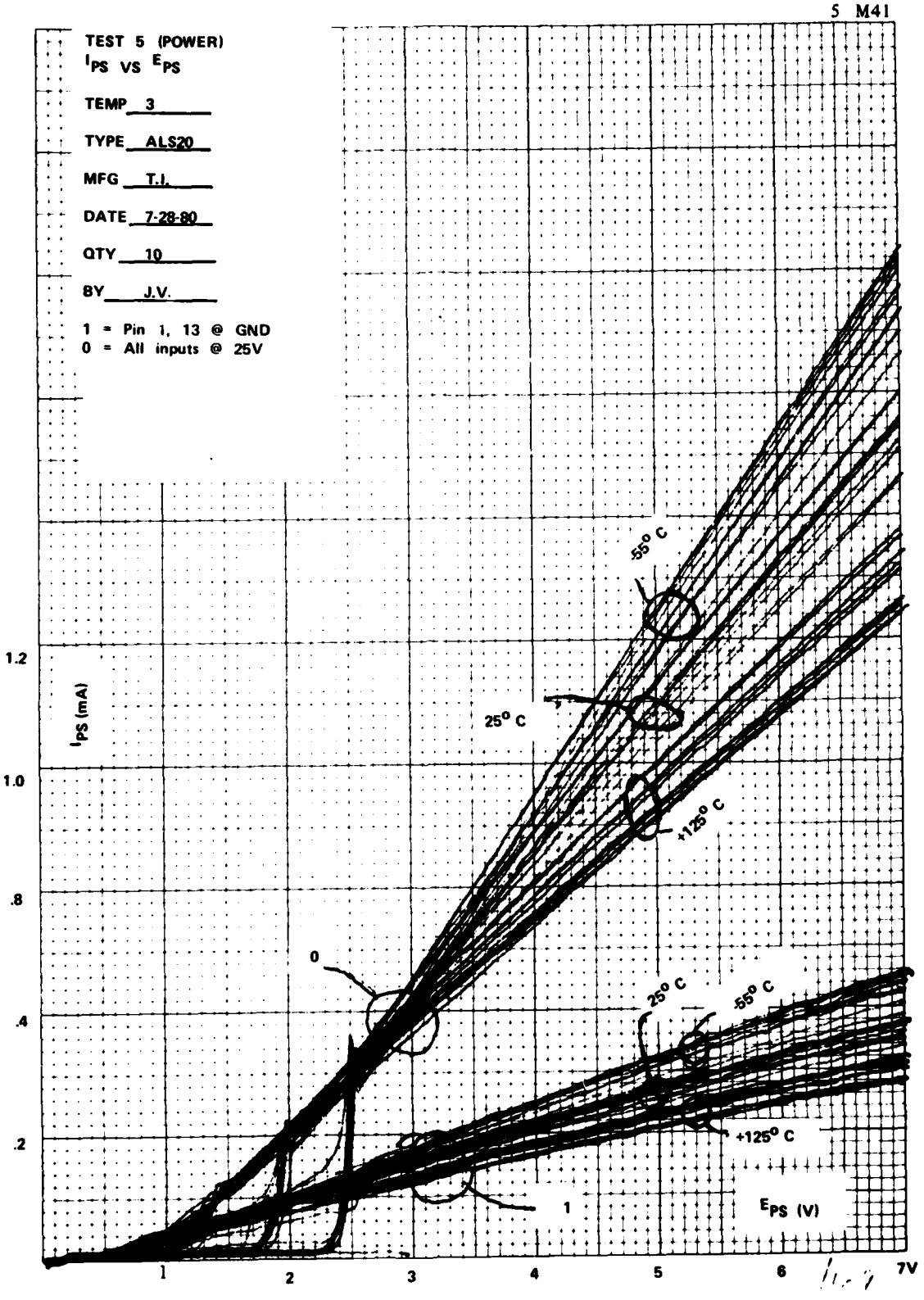

4A M41
TEST 4A VCC 5.5V
I_{IN} VS E_{IN} (0)
TEMP 3
TYPE ALS11
MFR T.I.
QTY 10
DATE 7-30-80
BY J.V.
Pin 1
I_{IN} (μA)
E_{IN} (V)
-55° C
25° C
+125° C
28
24
20
16
12
8
4
2V
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2

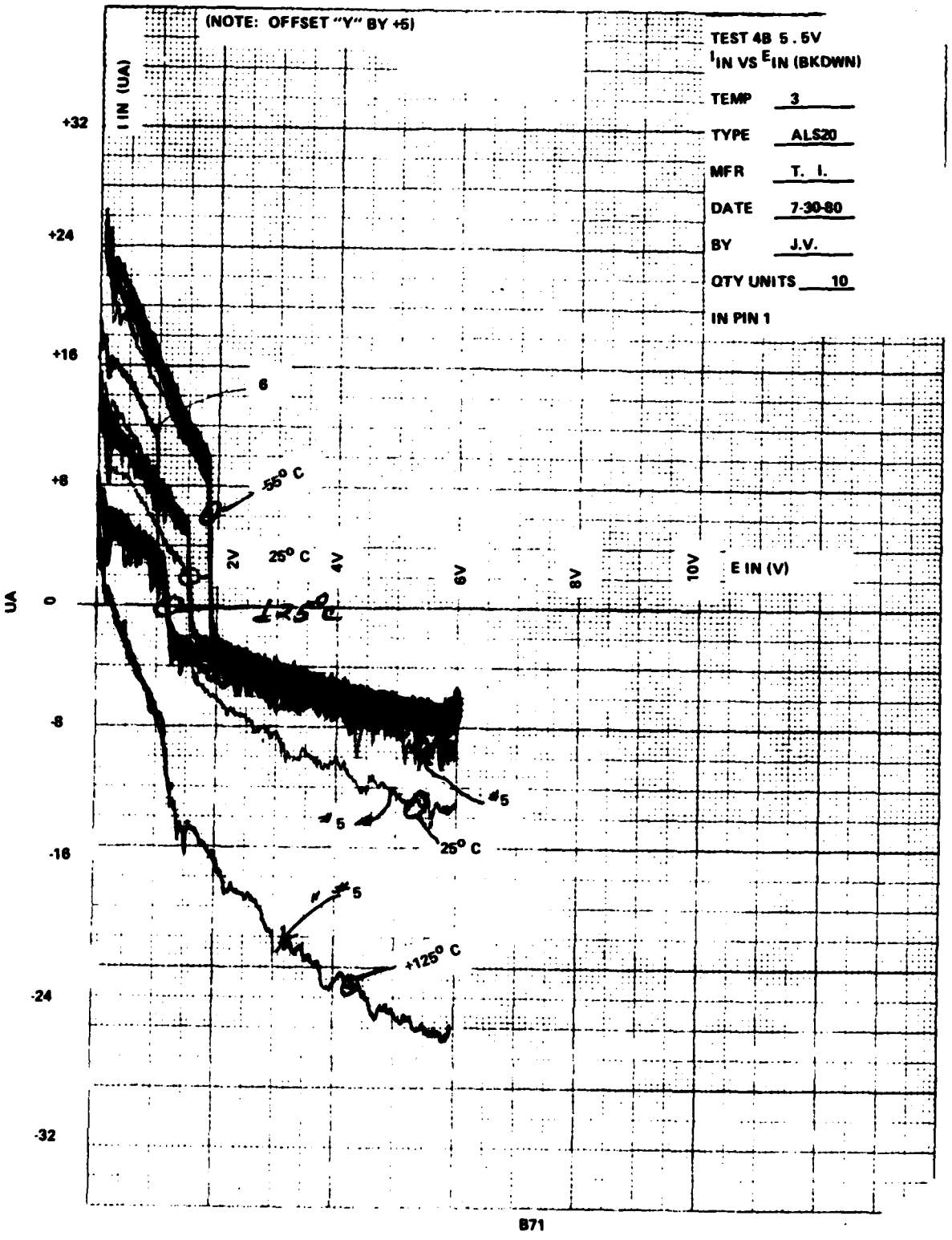

TEST 3 (VCC 4.5V)
E_{OUT} VS E_{IN}
TEMP 3
TYPE ALS 11
MFR TI
DATE 7-31-80
QTY 10
BY J.V.
IN PIN 2
OUT PIN 12
E OUT (V)
E IN (V)
-55° C
25° C
+125° C
6
5
4
3
2
1
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0

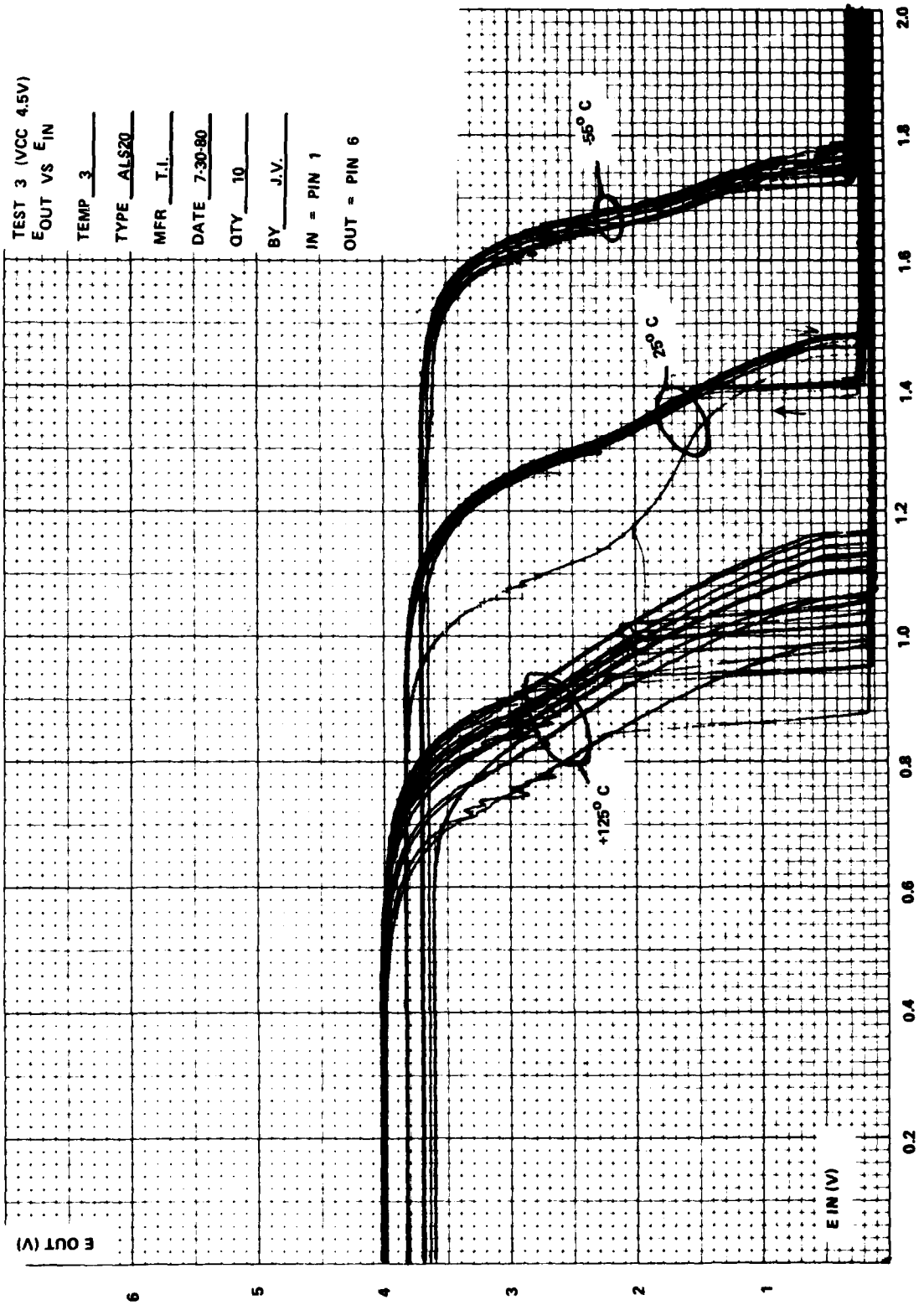

(NOTE: OFFSET "Y" BY +5)
TEST 4B 5.5
I_{IN} VS E_{IN} (BKDWN)
TEMP 3 °C
TYPE ALS11
MFR T.I.
DATE 7-30-80
BY J.V.
QTY UNITS 10
IN PIN 2
UA
+16
+12
+8
+4
0
-4
-8
-12
-16
25° C
-55° C
+125° C
4V
6V
8V
10V
E IN (V)

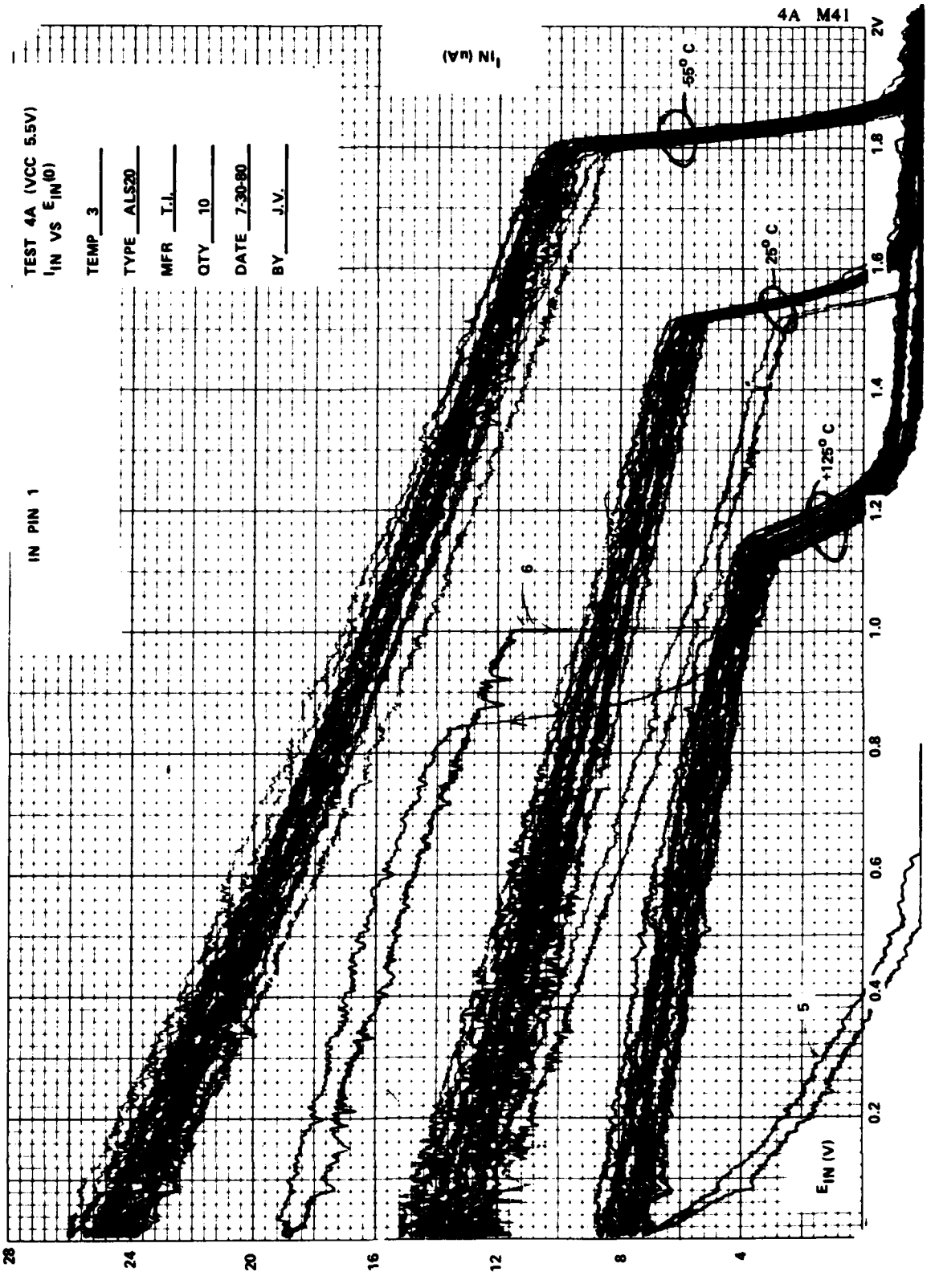

1A M41
TEST 1A VCC 4.5V
I_{OUT} VS E_{OUT} (0)
TEMP 3
TYPE ALS20
MFR TI
DATE 7-30-80
QTY 10
BY J.V.
OUTPUT PIN 6
40
32
24
16
8
I_{OUT} (mA)
+125° C
25° C
-55° C
E_{OUT} (V)
0.5
1.0
1.5
2.0
2.5
3.0
3.5V

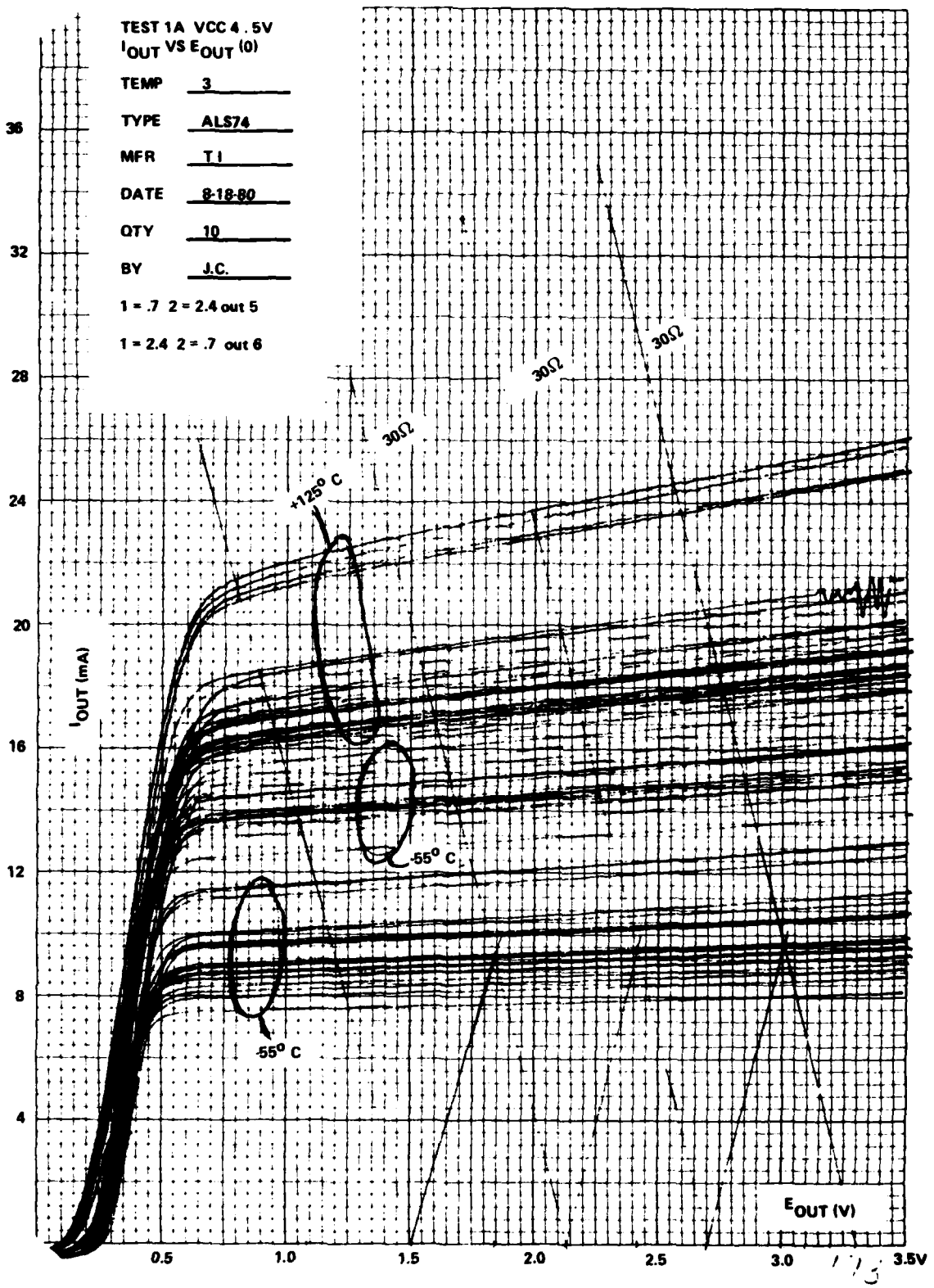

TEST 2 (VCC 5.5V)
I_{OUT} VS E_{OUT}(1)
TEMP 3
TYPE ALS20
MFR T.I.
DATE 7-30-80
BY J.V.
QTY 10
OUTPUT PIN 6
100
DA
90
80
70
60
50
40
30
20
10
I_{OUT} (MA)
+125°C
25° C
+125° C
-55° C
E_{OUT} (V)
+
1
2
3
4
5
6
7V
M41

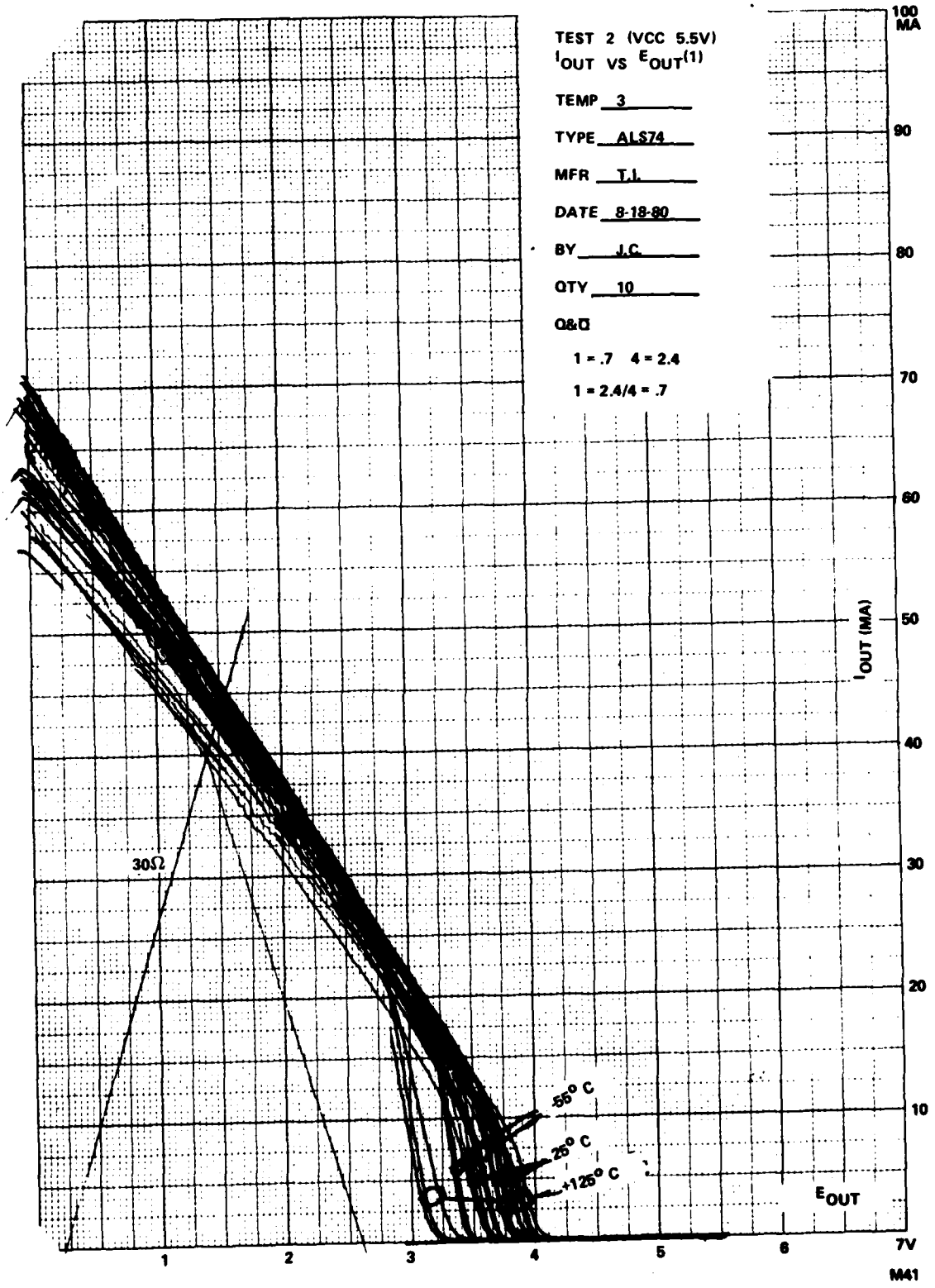

TEST 5 (POWER)
I_{PS} VS E_{PS}
TEMP 3
TYPE ALS20
MFG T.I.
DATE 7-28-80
QTY 10
BY J.V.
1 = Pin 1, 13 @ GND
0 = All inputs @ 25V
I_{PS} (mA)
1.2
1.0
.8
.4
.2
1
2
3
4
5
6
7V
E_{PS} (V)
-55° C
25° C
+125° C
0
25° C
-55° C
+125° C
1

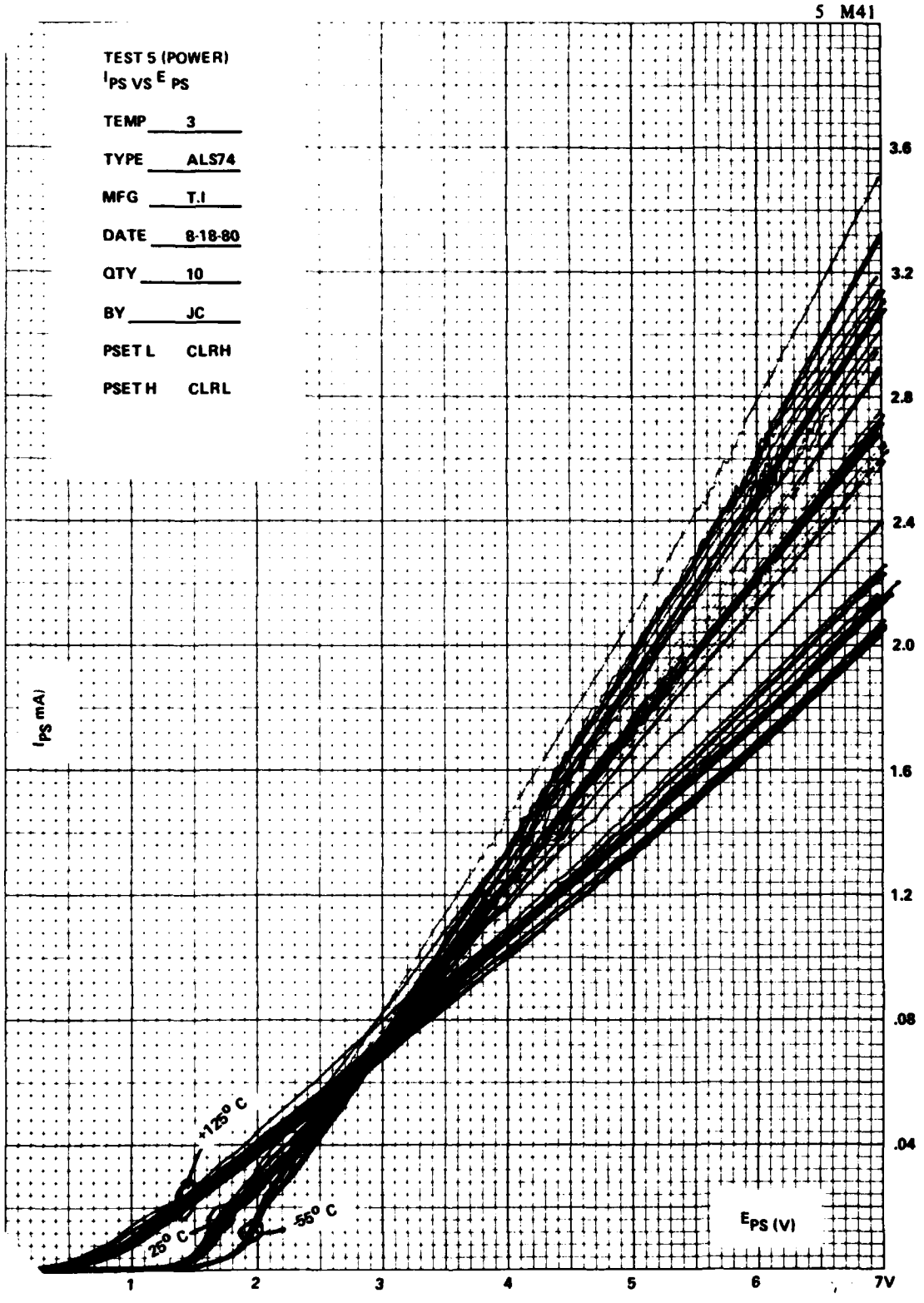

(NOTE: OFFSET "Y" BY +5)
TEST 4B 5.5V
I IN VS E IN (BKDWN)
TEMP 3
TYPE ALS20
MFR T. I.
DATE 7-30-80
BY J.V.
QTY UNITS 10
IN PIN 1
I IN (UA)
+32
+24
+16
+8
0
-8
-16
-24
-32
UA
2V
4V
6V
8V
10V
E IN (V)
6
-55° C
25° C
125° C
5
5
25° C
5
+125° C
B71

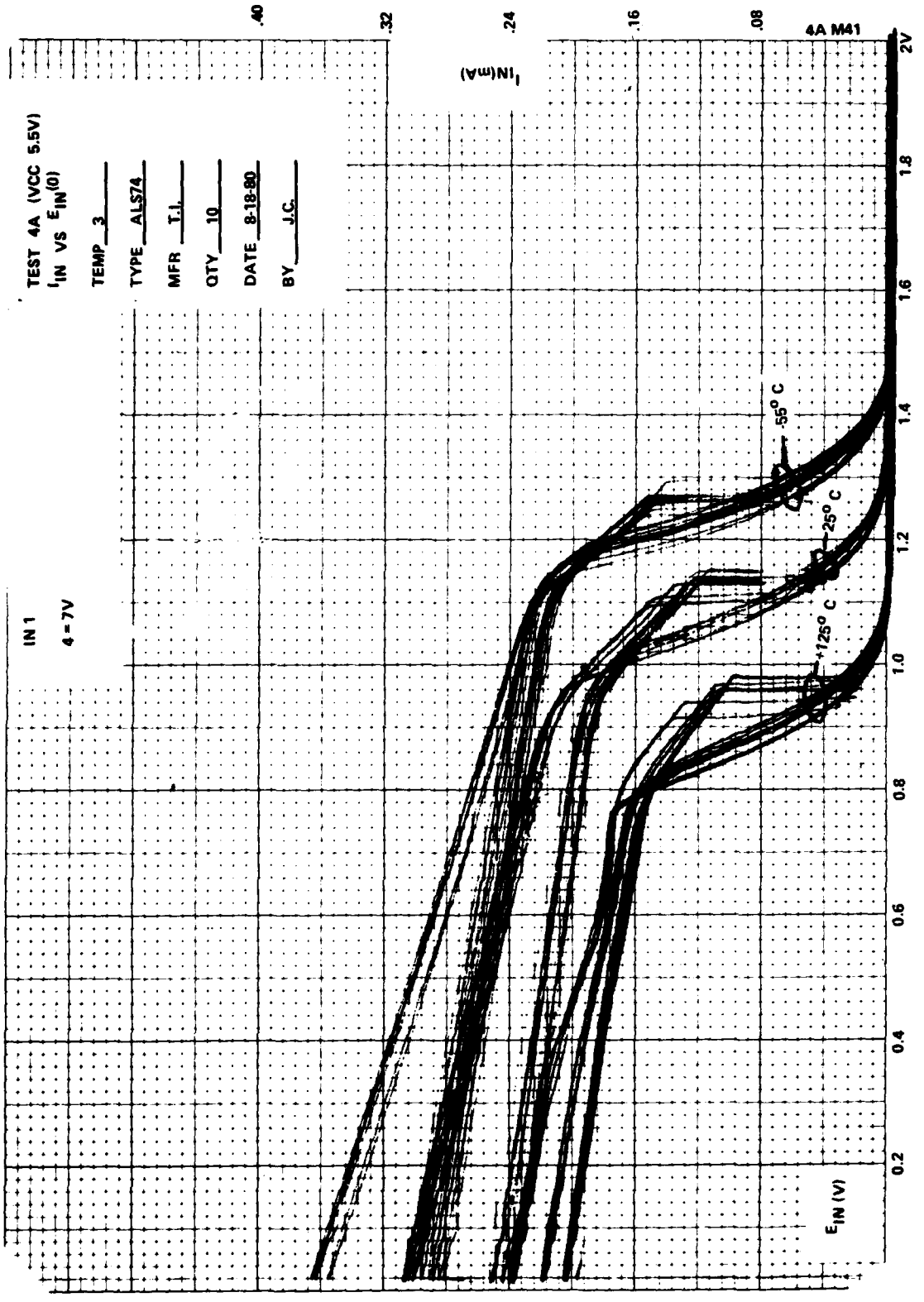

TEST 3 (VCC 4.5V)
E_{OUT} VS E_{IN}
TEMP 3
TYPE ALS20
MFR T.I.
DATE 7-30-80
QTY 10
BY J.V.
IN = PIN 1
OUT = PIN 6
-55° C
25° C
+125° C
E OUT (V)
E IN (V)
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
1
2
3
4
5
6

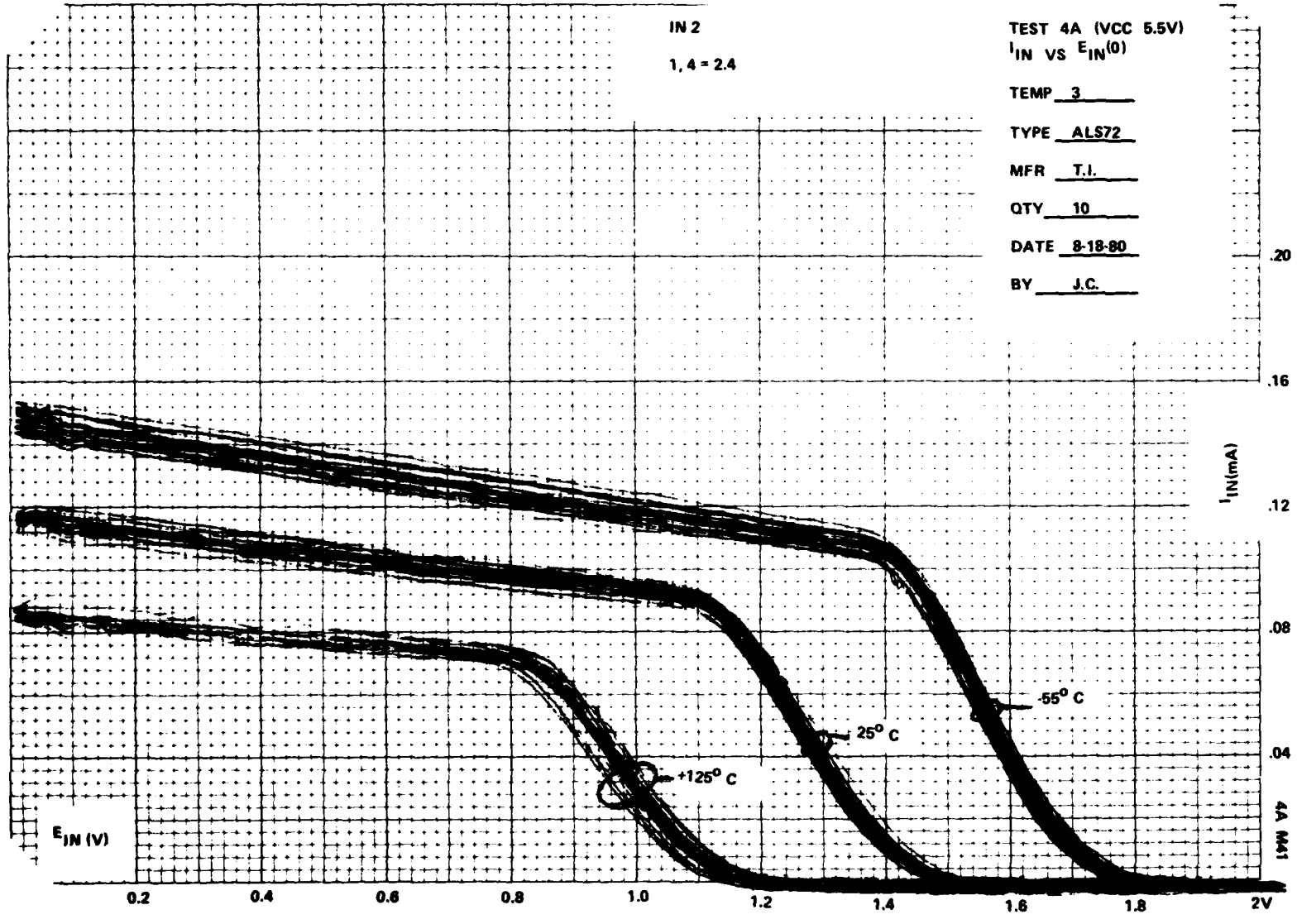

4A M41
TEST 4A (VCC 5.5V)
I_{IN} VS E_{IN}(0)
TEMP 3
TYPE ALS20
MFR T.I.
QTY 10
DATE 7-30-80
BY J.V.
IN PIN 1
I_{IN} (μA)
E_{IN} (V)
-55° C
25° C
+125° C
28
24
20
16
12
8
4
2V
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
6
5

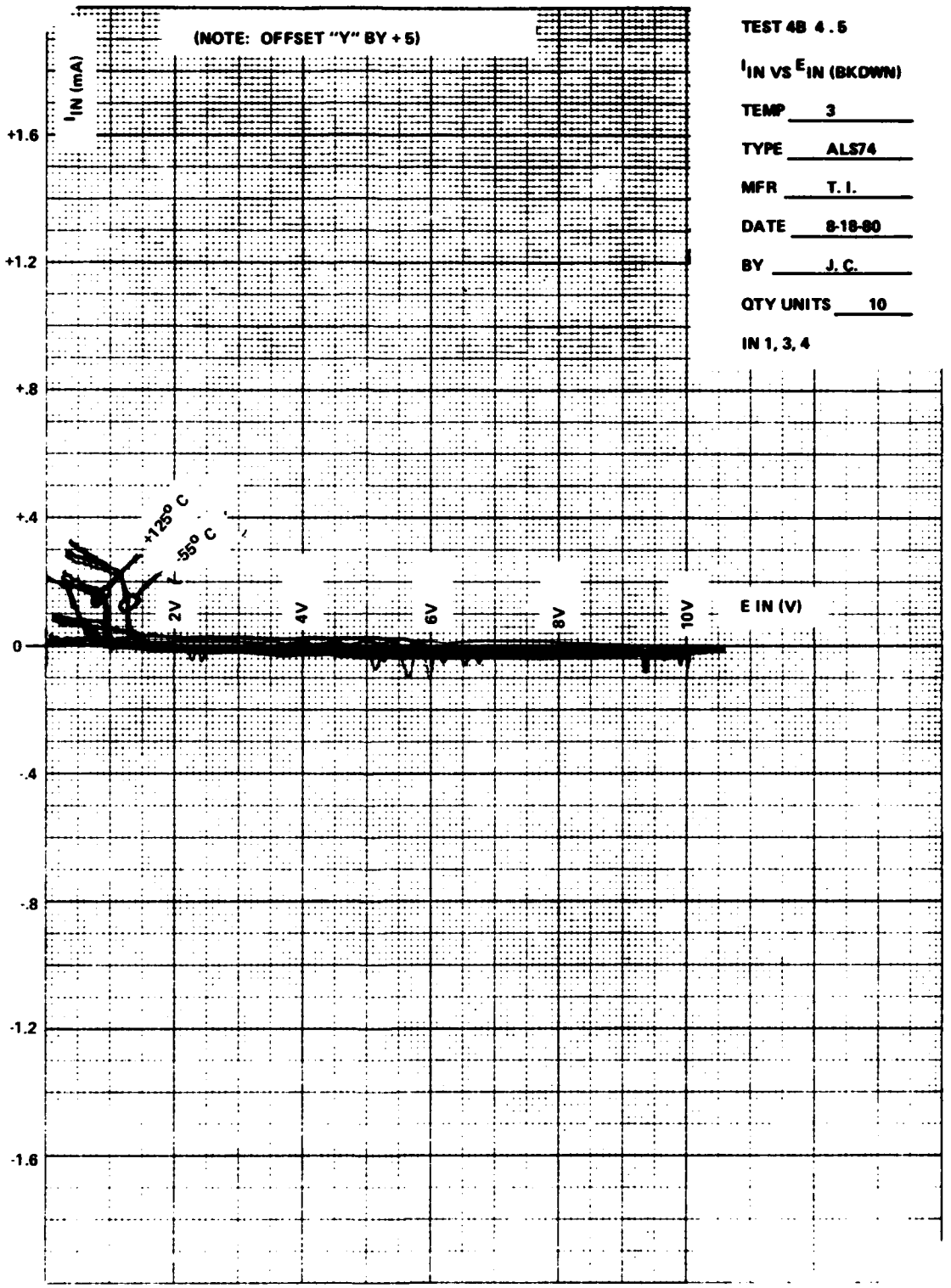

TEST 1A VCC 4 .5V
I_{OUT} VS E_{OUT} (0)
TEMP 3
TYPE ALS74
MFR T I
DATE 8-18-80
QTY 10
BY J.C.
1 = .7 2 = 2.4 out 5
1 = 2.4 2 = .7 out 6
36
32
28
24
20
16
12
8
4
I_{OUT} (mA)
30Ω
30Ω
30Ω
+125° C
-55° C
-55° C
0.5
1.0
1.5
2.0
2.5
3.0
3.5V
E_{OUT} (V)

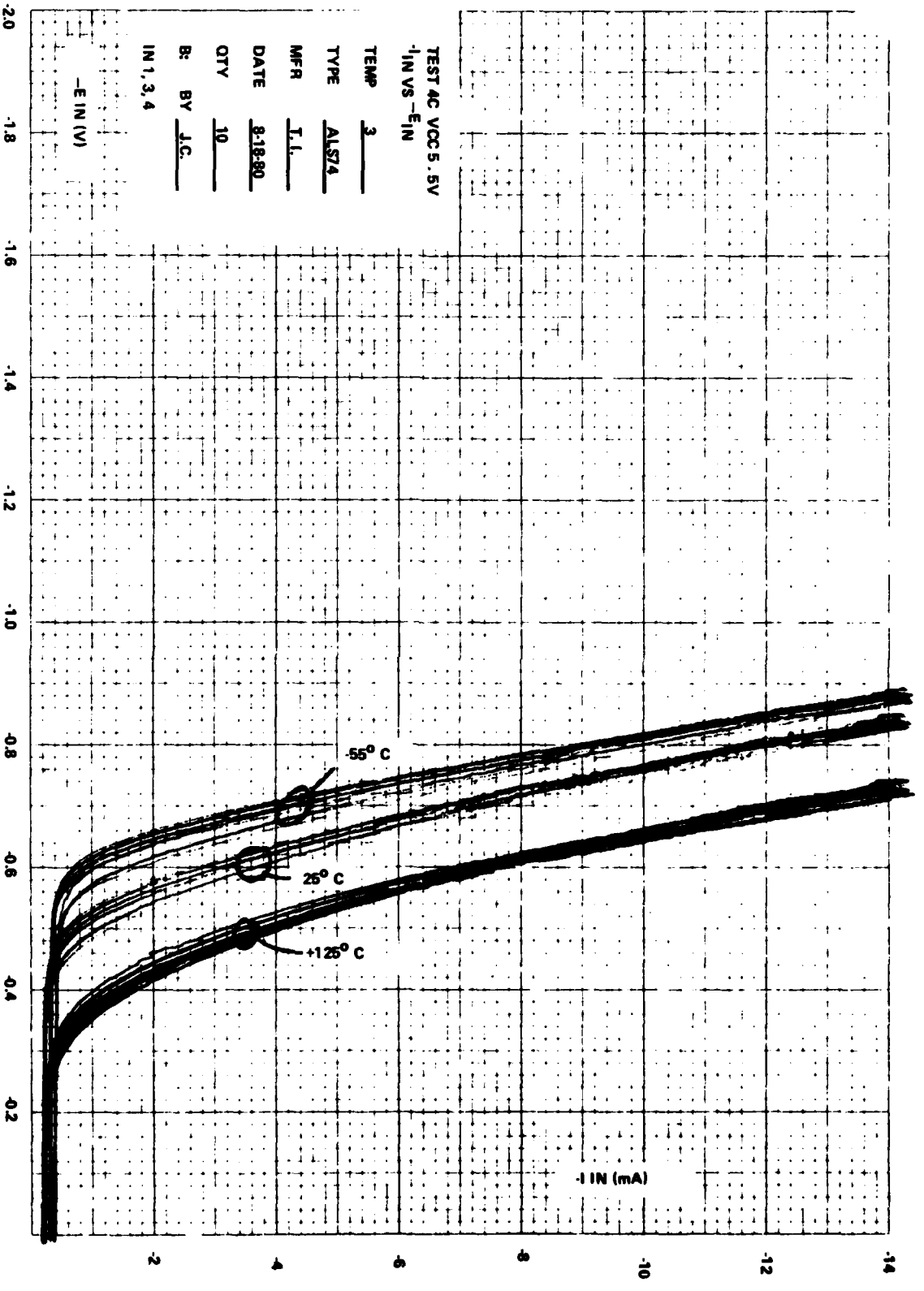

TEST 2 (VCC 5.5V)
I_{OUT} VS E_{OUT}(1)
TEMP 3
TYPE ALS74
MFR T.I.
DATE 8-18-80
BY J.C.
QTY 10
Q&D
1 = .7 4 = 2.4
1 = 2.4/4 = .7
100 MA
90
80
70
60
50
40
30
20
10
I_{OUT} (MA)
30Ω
-55° C
25° C
+125° C
E_{OUT}
1
2
3
4
5
6
7V
M41

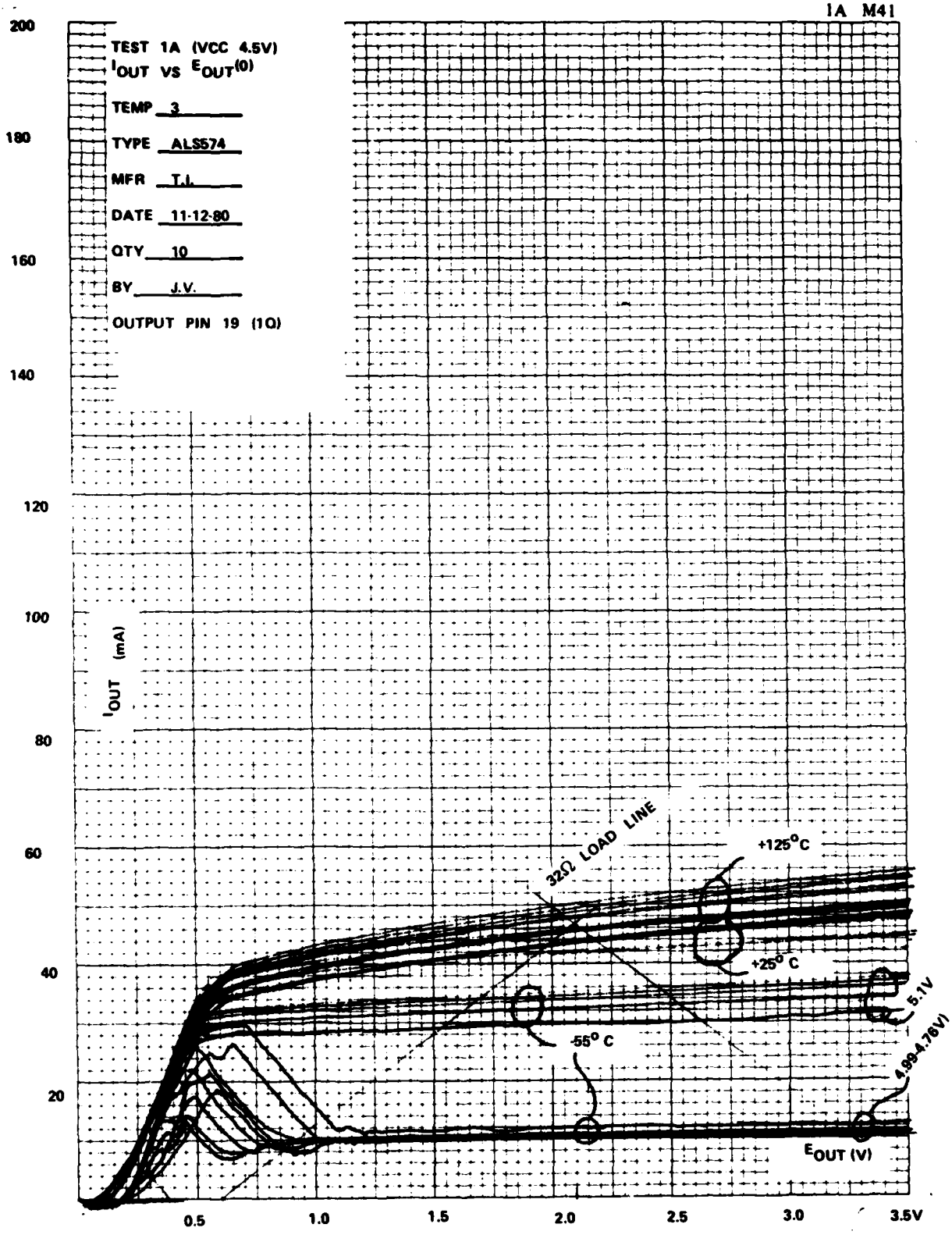

5 M41
TEST 5 (POWER)
I_{PS} VS E_{PS}
TEMP 3
TYPE ALS74
MFG T.I
DATE 8-18-80
QTY 10
BY JC
PSET L CLRH
PSET H CLRL
I_{PS} mA)
3.6
3.2
2.8
2.4
2.0
1.6
1.2
.08
.04
+125° C
25° C
-55° C
E_{PS} (V)
1
2
3
4
5
6
7V

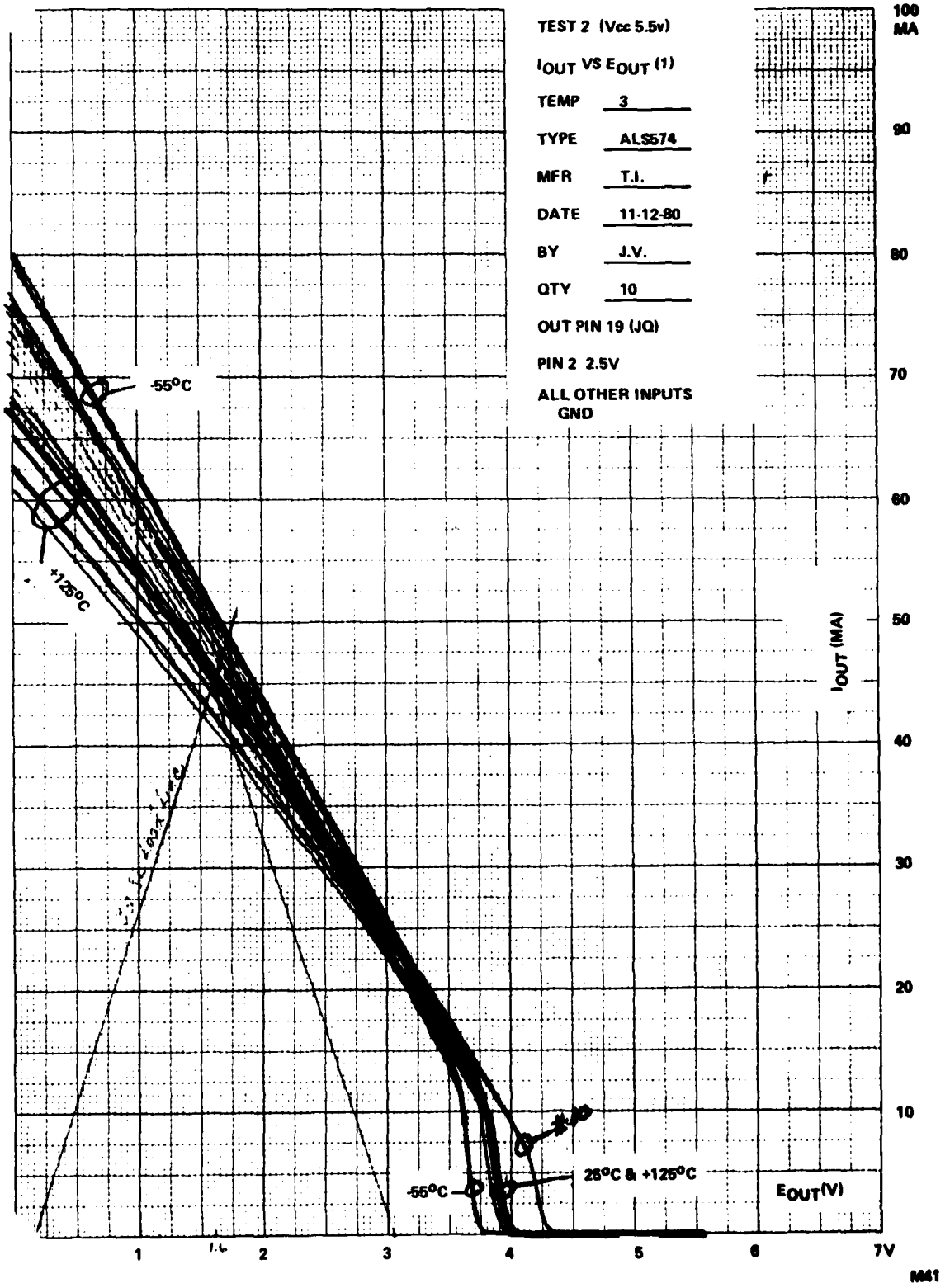

TEST 4A (VCC 5.5V)
I_{IN} VS $E_{IN}(0)$
TEMP 3
TYPE ALS74
MFR T.I.
QTY 10
DATE 8-18-80
BY J.C.
IN 1
4 = 7V
4A M41
I_{IN}(mA)
E_{IN} (V)
-55° C
-25° C
+125° C
.40
.32
.24
.16
.08
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2V


IN 2
1, 4 = 2.4
TEST 4A (VCC 5.5V)
I_{IN} VS $E_{IN(0)}$
TEMP 3
TYPE ALS72
MFR T.I.
QTY 10
DATE 8-18-80
BY J.C.
.20
.16
.12
.08
.04
I_{IN}(mA)
-55° C
25° C
+125° C
E_{IN} (V)
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2V
4A M41

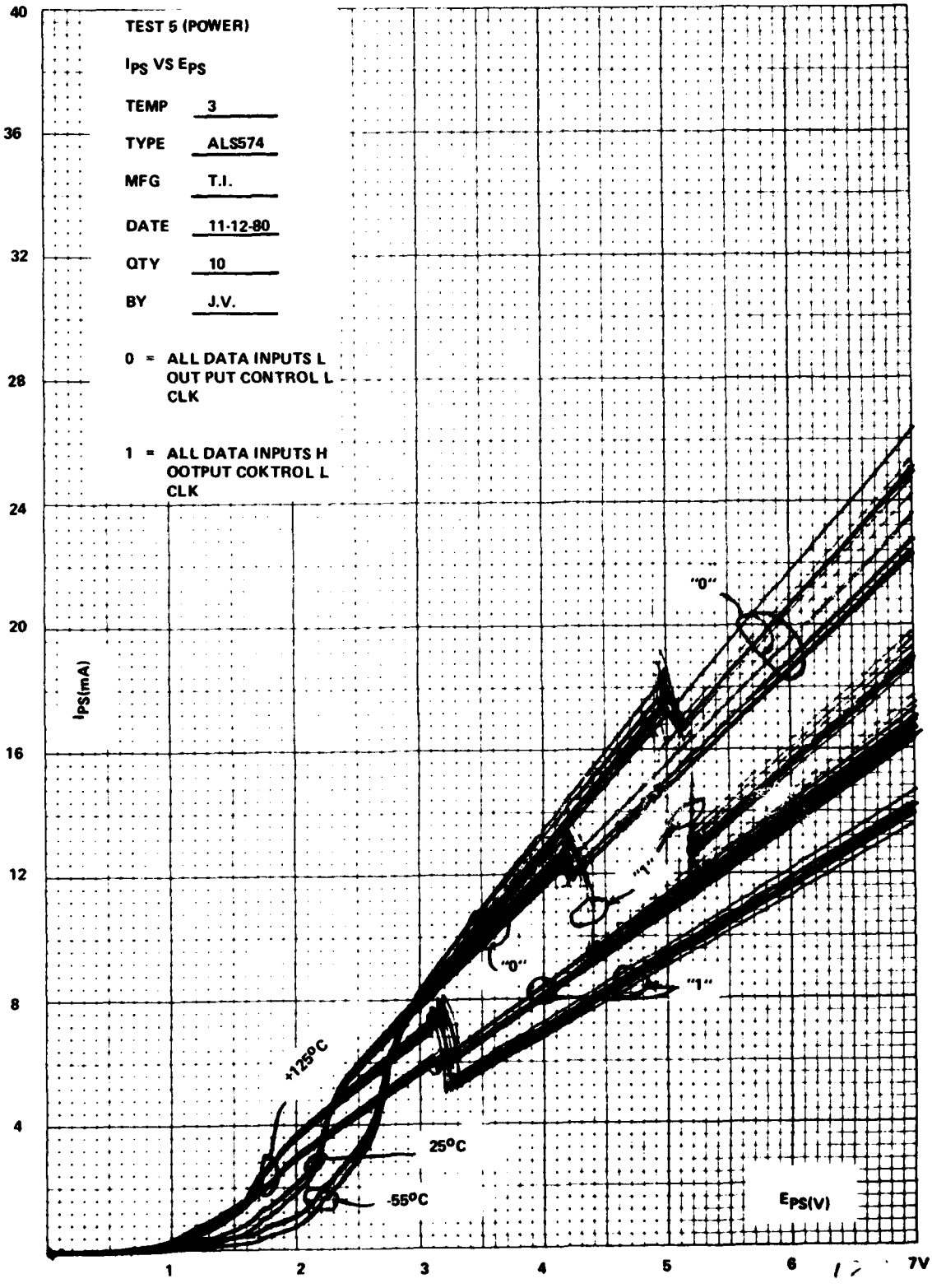

(NOTE: OFFSET "Y" BY + 5)
TEST 4B 4.5
I_{IN} VS E_{IN} (BKDWN)
TEMP 3
TYPE ALS74
MFR T. I.
DATE 8-18-80
BY J. C.
QTY UNITS 10
IN 1, 3, 4
I_{IN} (mA)
+1.6
+1.2
+.8
+.4
0
-.4
-.8
-1.2
-1.6
+125° C
-55° C
2V
4V
6V
8V
10V
E IN (V)

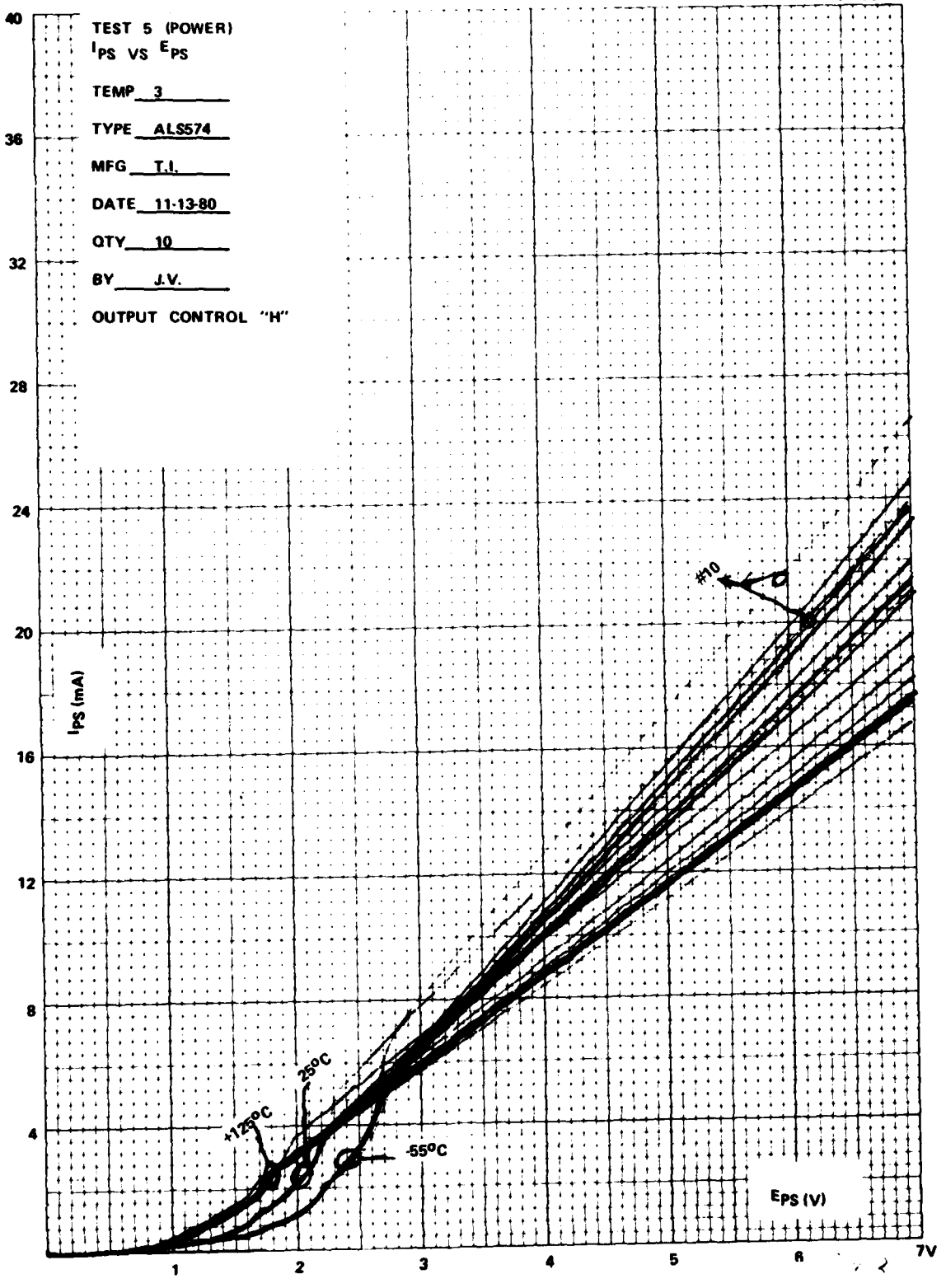

TEST 4C VCC 5.5V
-I_IN VS -E_IN
TEMP 3
TYPE ALS74
MFR T.I.
DATE 8-18-80
QTY 10
B: BY J.C.
IN 1, 3, 4
-55° C
25° C
+125° C
-I IN (mA)
-E IN (V)
-2.0
-1.8
-1.6
-1.4
-1.2
-1.0
-0.8
-0.6
-0.4
-0.2
-2
-4
-6
-8
-10
-12
-14

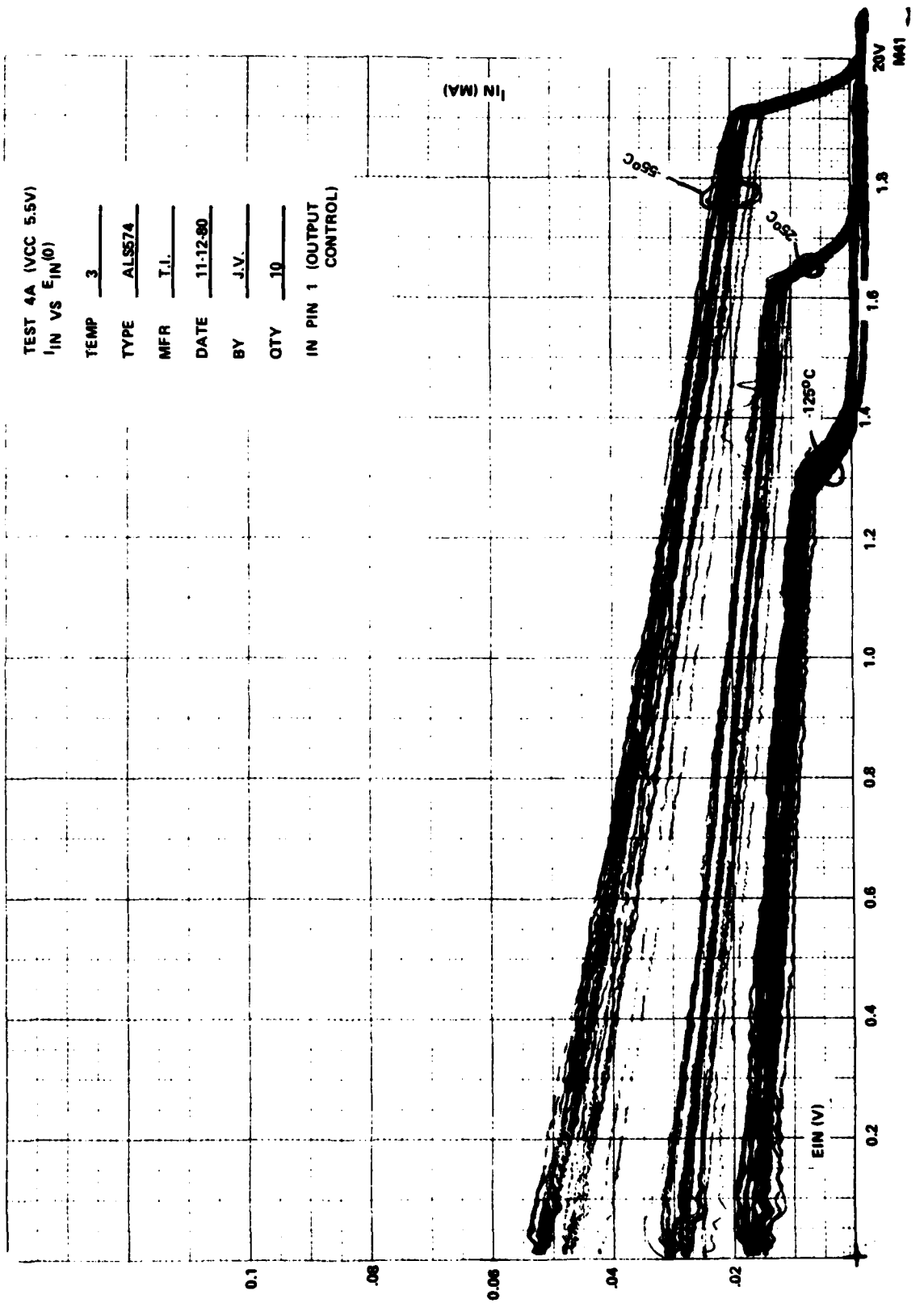

TEST 1A (VCC 4.5V)
I_{OUT} VS E_{OUT}(0)
TEMP 3
TYPE ALS574
MFR T.I.
DATE 11-12-80
QTY 10
BY J.V.
OUTPUT PIN 19 (1Q)
200
180
160
140
120
100
80
60
40
20
I_{OUT} (mA)
32Ω LOAD LINE
+125° C
+25° C
-55° C
5.1V
4.99-4.76V
E_{OUT} (V)
0.5
1.0
1.5
2.0
2.5
3.0
3.5V

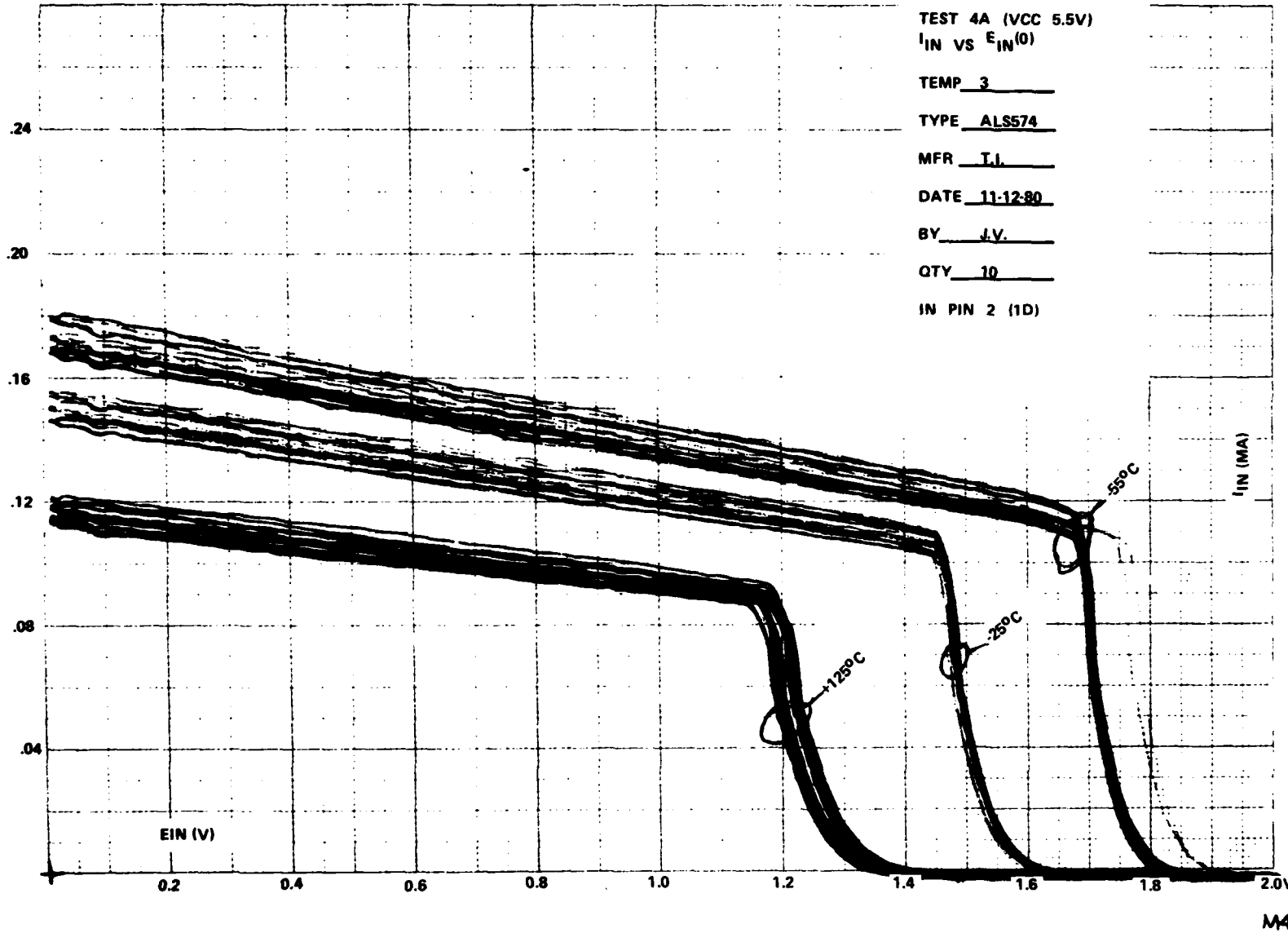

TEST 2 (Vcc 5.5v)
I_{OUT} VS E_{OUT} (1)
TEMP 3
TYPE ALS574
MFR T.I.
DATE 11-12-80
BY J.V.
QTY 10
OUT PIN 19 (JQ)
PIN 2 2.5V
ALL OTHER INPUTS GND
-55°C
+125°C
25°C & +125°C
-55°C
I_{OUT} (MA)
E_{OUT}(V)
100 MA
90
80
70
60
50
40
30
20
10
1
2
3
4
5
6
7V
M41

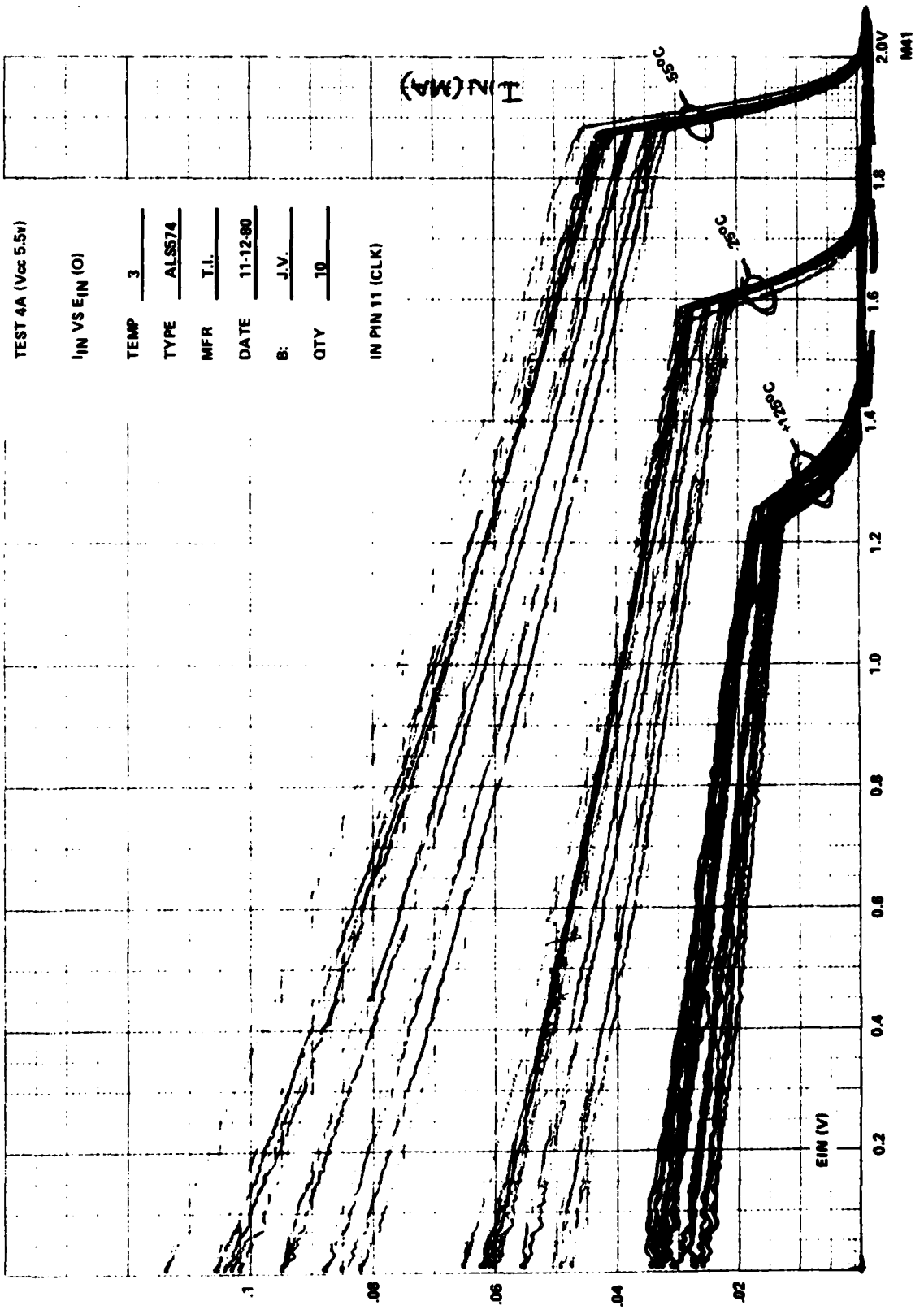
5M41

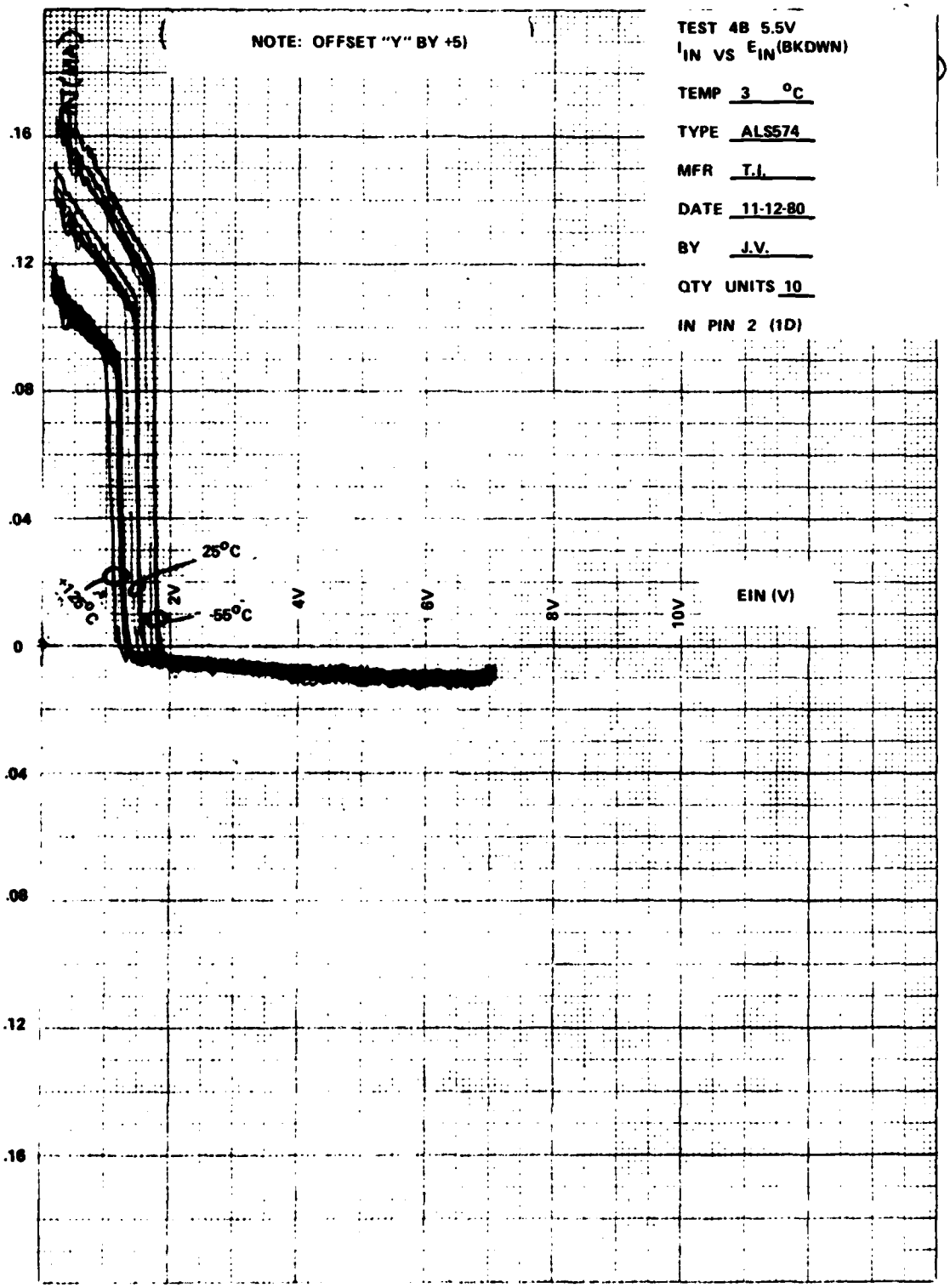

TEST 5 (POWER)
I_{PS} VS E_{PS}
TEMP 3
TYPE ALS574
MFG T.I.
DATE 11-12-80
QTY 10
BY J.V.
0 = ALL DATA INPUTS L
OUT PUT CONTROL L
CLK
1 = ALL DATA INPUTS H
OOTPUT COKTROL L
CLK
$I_{PS(mA)}$
$E_{PS(V)}$
"0"
"1"
"0"
"1"
+125°C
25°C
-55°C
40
36
32
28
24
20
16
12
8
4
1
2
3
4
5
6
7V

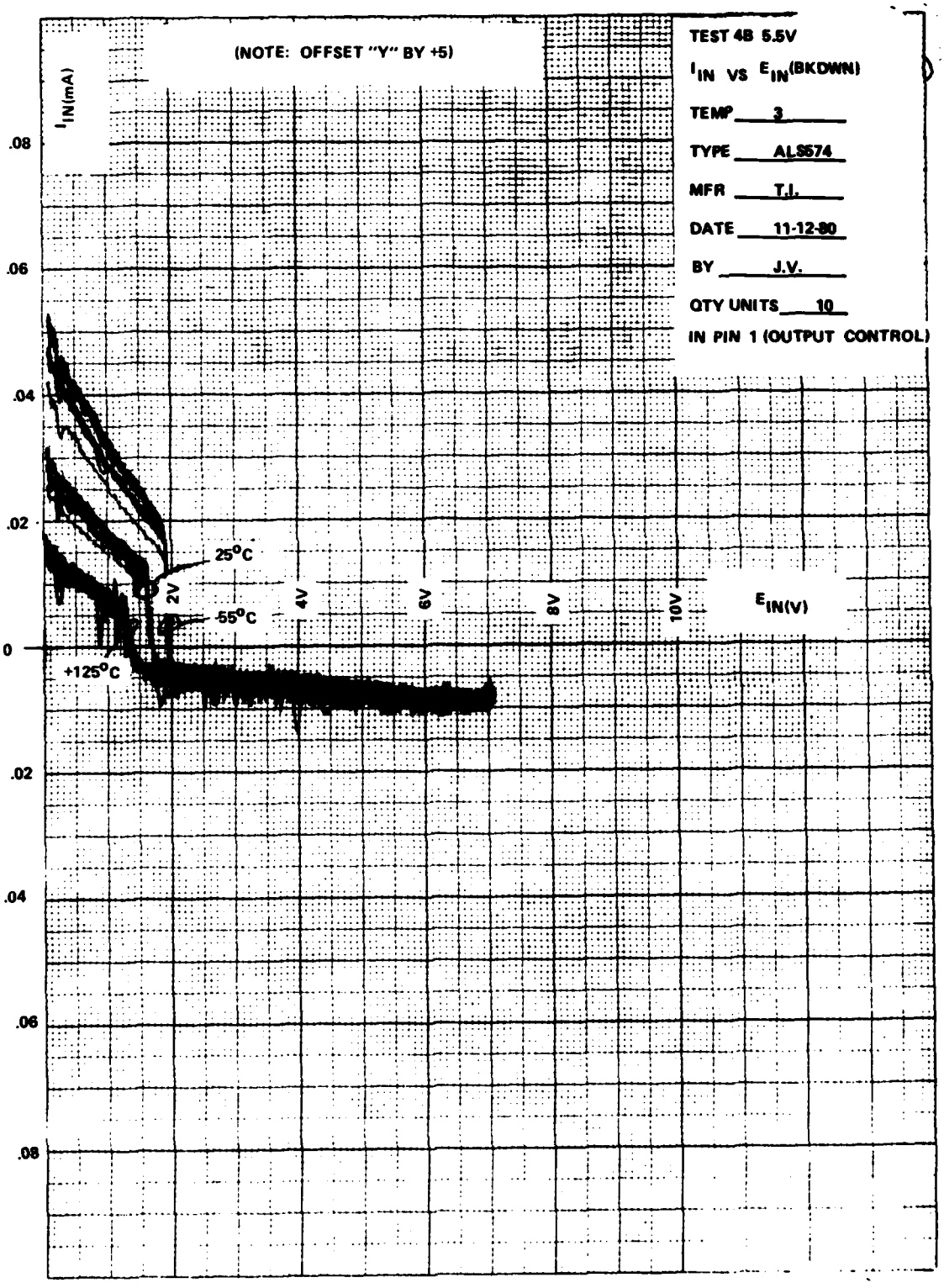

TEST 5 (POWER)
I_{PS} VS E_{PS}
TEMP 3
TYPE ALS574
MFG T.I.
DATE 11-13-80
QTY 10
BY J.V.
OUTPUT CONTROL "H"
40
36
32
28
24
20
16
12
8
4
I_{PS} (mA)
#10
+125°C
25°C
-55°C
E_{PS} (V)
1
2
3
4
5
6
7V

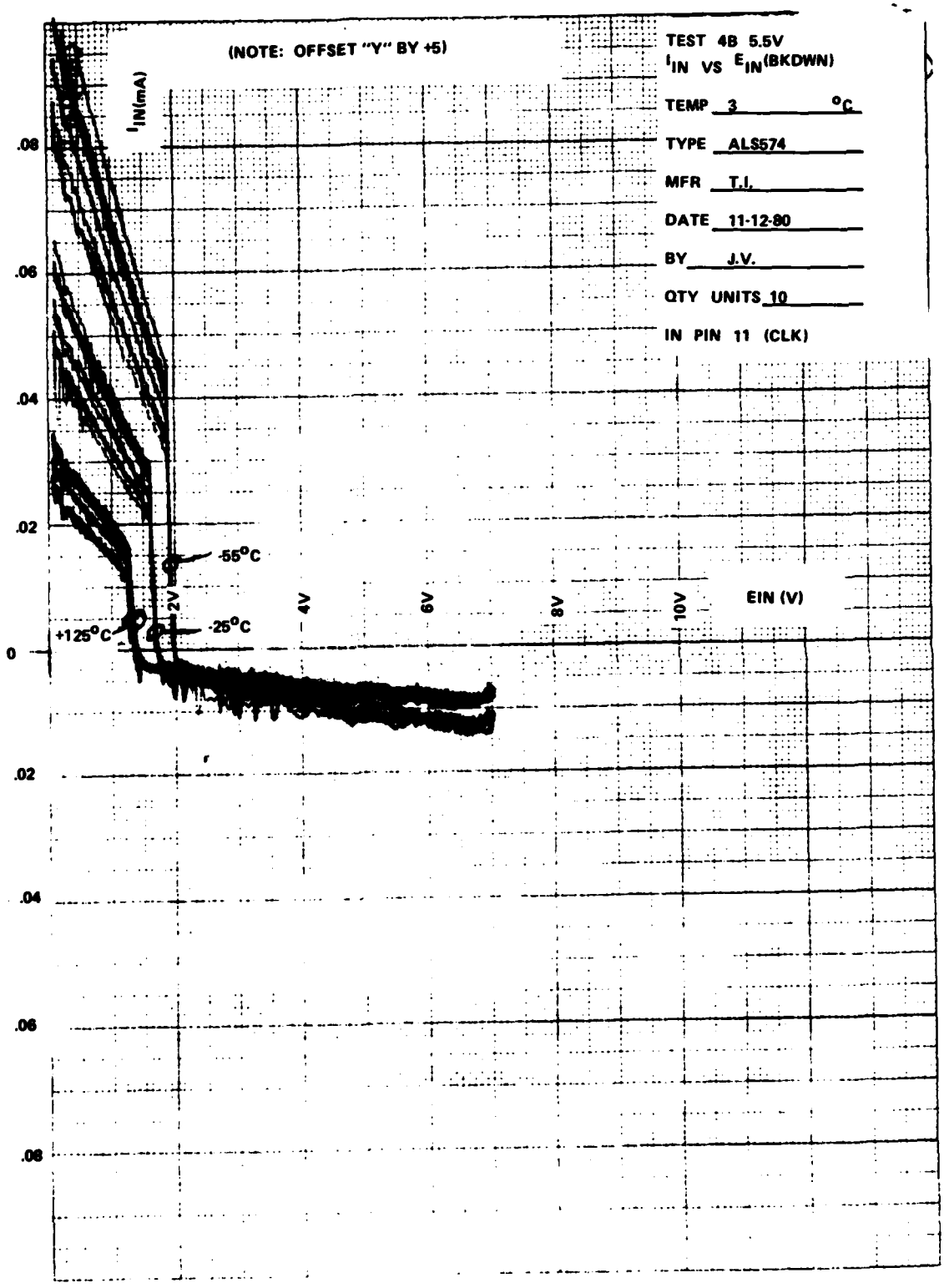

TEST 4A (VCC 5.5V)
I_{IN} VS E_{IN}(0)
TEMP 3
TYPE ALS574
MFR T.I.
DATE 11-12-80
BY J.V.
QTY 10
IN PIN 1 (OUTPUT CONTROL)
I_{IN} (MA)
EIN (V)
-55°C
-25°C
125°C
20V
M41


TEST 4A (VCC 5.5V)
I_{IN} VS $E_{IN}(0)$
TEMP 3
TYPE ALS574
MFR T.I.
DATE 11-12-80
BY J.V.
QTY 10
IN PIN 2 (1D)
.24
.20
.16
.12
.08
.04
I_{IN} (MA)
-55°C
25°C
125°C
EIN (V)
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0V


TEST 4A (Vcc 5.5v)
I_{IN} VS E_{IN} (O)
TEMP 3
TYPE ALS574
MFR T.I.
DATE 11-12-80
B: J.V.
QTY 10
IN PIN 11 (CLK)
I_{IN}(MA)
EIN (V)
-55°C
+25°C
+125°C
2.0V
M41


NOTE: OFFSET "Y" BY +5)
TEST 4B 5.5V
I_{IN} VS E_{IN}(BKDWN)
TEMP 3 °C
TYPE ALS574
MFR T.I.
DATE 11-12-80
BY J.V.
QTY UNITS 10
IN PIN 2 (1D)
.16
.12
.08
.04
0
.04
.08
.12
.16
25°C
-55°C
2V
4V
6V
8V
10V
EIN (V)


(NOTE: OFFSET "Y" BY +5)
TEST 4B 5.5V
I_{IN} VS E_{IN}(BKDWN)
TEMP 3
TYPE ALS574
MFR T.I.
DATE 11-12-80
BY J.V.
QTY UNITS 10
IN PIN 1 (OUTPUT CONTROL)
I_{IN}(mA)
.08
.06
.04
.02
0
.02
.04
.06
.08
25°C
-55°C
+125°C
2V
4V
6V
8V
10V
$E_{IN(V)}$


(NOTE: OFFSET "Y" BY +5)
TEST 4B 5.5V
I_{IN} VS E_{IN}(BKDWN)
TEMP 3 °C
TYPE ALS574
MFR T.I.
DATE 11-12-80
BY J.V.
QTY UNITS 10
IN PIN 11 (CLK)
I_{IN}(mA)
.08
.06
.04
.02
0
.02
.04
.06
.08
2V
4V
6V
8V
10V
EIN (V)
-55°C
+125°C
-25°C

MISSION
of
Rome Air Development Center

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